ARL-TR-10088 ● APR 2025

Advanced Radar Waveform Generator Two-Channel Upgrade

by William Diehl and Prosper Adangwa

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DEVCOM Army Research Laboratory

REPORT DOCUMENTATION PAGE

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED	
		START DATE	END DATE
April 2025	Technical Report	9/01/2024	3/27/2025

4. TITLE AND SUBTITLE
Advanced Radar Waveform Generator Two-Channel Upgrade

5a. CONTRACT NUMBER	5b. GRANT NUMBER	5c. PROGRAM ELEMENT NUMBER
5d. PROJECT NUMBER	**5e. TASK NUMBER**	**5f. WORK UNIT NUMBER**

6. AUTHOR(S)
William Diehl and Prosper Adangwa

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
DEVCOM Army Research Laboratory ATTN: FCDD-RLB-ST Adelphi, MD 20783-1138	ARL-TR-10088

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
DISTRIBUTION STATEMENT A. Approved for public release: distribution unlimited.

13. SUPPLEMENTARY NOTES
ORCID: William Diehl, 0000-0002-6293-5018

14. ABSTRACT
This report introduces the Advanced Radar Waveform Generator Two-Channel Upgrade (ARWG-2). The ARWG-2 is implemented in the commercial AMD-Xilinx Gen3 RF system-on-chip in the ZCU208 Evaluation Board form factor. It provides a flexible platform for generating user-defined radar pulses with complex features such as intrapulse modulations, near real-time custom waveform generation, pulse-to-pulse frequency agility, user-defined amplitude, frequency and phase modulation, and composite pulse group generation. It includes multiple user interfaces including serial command line interface and Python-based graphical user interface. The ARWG is connected to a supporting PC via a Gigabit Ethernet interface and can therefore interact with powerful applications residing in PCs or across networks. This upgrade increases the capacity of the generator from its previous single-channel design to a two-channel design.

15. SUBJECT TERMS
electromagnetic warfare, radar, software-defined radio, field-programmable gate array, FPGA, RF, system-on-chip, Electromagnetic Spectrum Sciences

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES
a. REPORT	b. ABSTRACT	C. THIS PAGE		
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UU	22

19a. NAME OF RESPONSIBLE PERSON	19b. PHONE NUMBER *(Include area code)*
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STANDARD FORM 298 (REV. 5/2020)
Prescribed by ANSI Std. Z39.18

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1. Introduction

This report describes the update of the Advanced Radar Waveform Generator (ARWG)[1] from a single-channel to a two-channel version called ARWG-2. The ARWG's capabilities are adequately described in Diehl and Tesny[1] and will not be restated in this report. Rather, this report details the capacity increase where all functions are now simultaneously present across two channels.

An original goal of the ARWG is to present user-programmable high-fidelity complex radar waveforms for research purposes, including novel signal detection and processing algorithms and artificial intelligence and machine learning (AI/ML) applications. Multichannel capability allows emulation of RF environments with "pulse-on-pulse" sequences, that is, the near simultaneous arrival of multiple uncorrelated radar pulses, which are especially challenging for signal processors such as deinterleavers and AI/ML signal classifiers. When ARWG is used to generate signals for open-air radiation, ARWG-2 enables transmittal of two simultaneous and independent emitters.

Aside from any technical innovations of ARWG-2, completion of this upgrade leveraged the Army's organizational innovation. Specifically, ARWG-2 was not developed at the U.S. Army Combat Capabilities Development Command Army Research Laboratory, but rather in the "Chimera Forge" Innovation Lab of the 2nd Multi-Domain Task Force (2MDTF) located in Mainz-Kastel, Germany. A fly-away semi-ruggedized version of the Generation (Gen) 3 RF system-on-chip (RFSoC) and Xilinx ZCU208 evaluation board and development environment was prepared and transported to Mainz-Kastel and was jointly installed and operated by 2MDTF Soldiers and DEVCOM Army Research Laboratory forward-deployed technical advisors. Evaluation of any RF-intensive product requires extensive test-and-measurement equipment to verify that proper signals are being generated at the many stages of design. This test-and-measurement was performed on the low-cost PicoScope 5000 oscilloscope and spectrum analyzer ($1200 per unit cost) and used 2MDTF's operational signal classification equipment. 2MDTF has been using ARWG, and now ARWG-2, for development of AI/ML signal classification models and generation of signals to simulate its own equipment for mission purposes. The integration of ARL and 2MDTF tools and personnel at a forward innovation lab is a highly successful Army organizational innovation and should be explored across the Army and explored for additional capabilities.

2. Two-Channel Design Overview

A single ARWG channel is depicted in Figure 1 and consists of four signal generators: a frequency modulation (FM) direct digital synthesizer (DDS) generator (FMGEN), a binary phase-shift-keyed generator (BPSKGEN) DDS, and two custom signal generators, or variable direct digital synthesizers (VARDDSs). FMGENs and BPSKGENs do not require any streaming input; their input comes from software through discrete parameters transmitted on an Advanced eXtensible Interface (AXI)-Lite interface. VARDDS do require periodic streaming inputs from direct memory access (DMA) via a specially designed selector. Either a single generator or null output is selected at a time per single channel. In addition to the generators, each channel has three modulators operating in series on the generated data stream: the phase, amplitude, and noise modulators. The generators and modulators are described in Diehl and Tesny.[1]

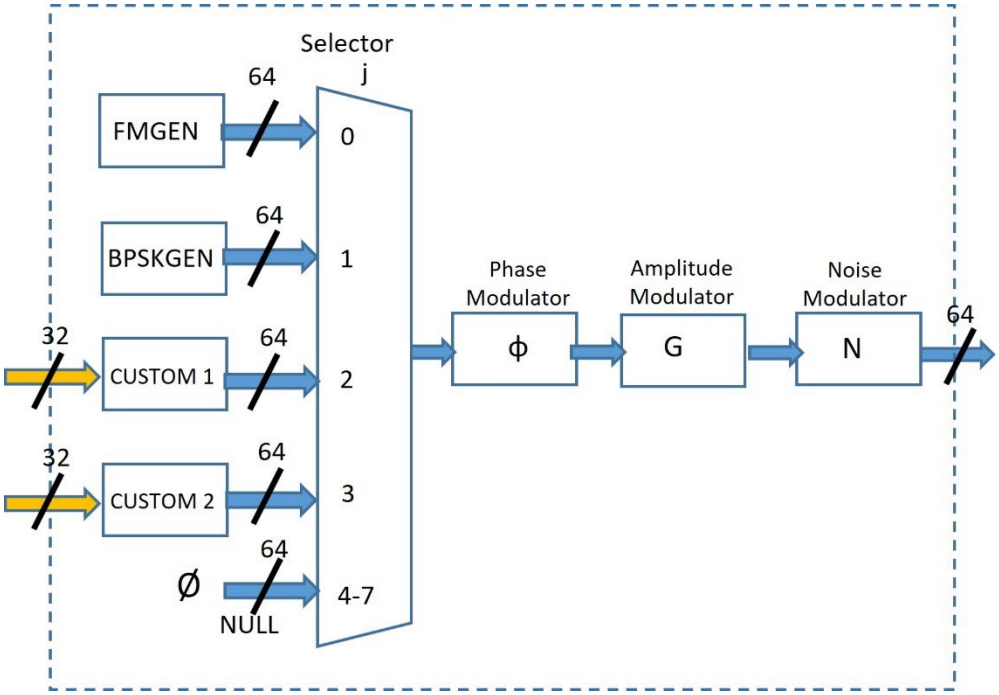

Figure 1. Single ARWG channel.

The composite ARWG-2 design consisting of two channels is shown in Figure 2. The DMA custom selector loads all four VARDDS instances across both channels. The output of Channel 1 (CH1) is hardwired to digital-to-analog converter (DAC) 228 and 230, and the output of Channel 2 (CH2) is hardwired to DAC 229 and 231. The wiring of channels to individual DACs is an arbitrary choice but is also determined by the composition of the ZCU208 XM655 daughter card and available balanced-to-unbalanced (balun). For example, each channel can output

simultaneously in two frequency bands: 10 MHz–1 GHz, or 1–4 GHz. Each numerically controlled oscillator (NCO) controller is connected to a unique DAC and independently controls the DAC output frequency. Additionally, there are five AXI Timers responsible for pulse group control.

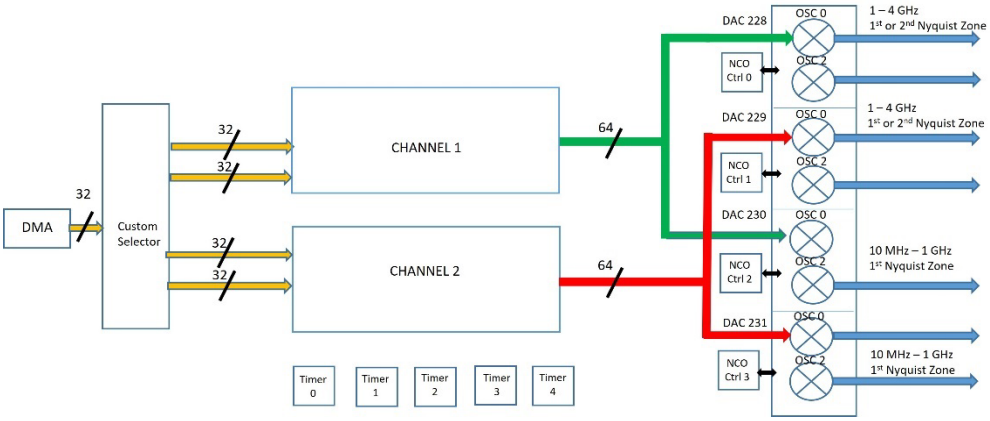

Figure 2. ARWG-2 composite overview.

A macro-level comparison of hardware block designs between ARWG and ARWG-2 is shown in Figure 3.

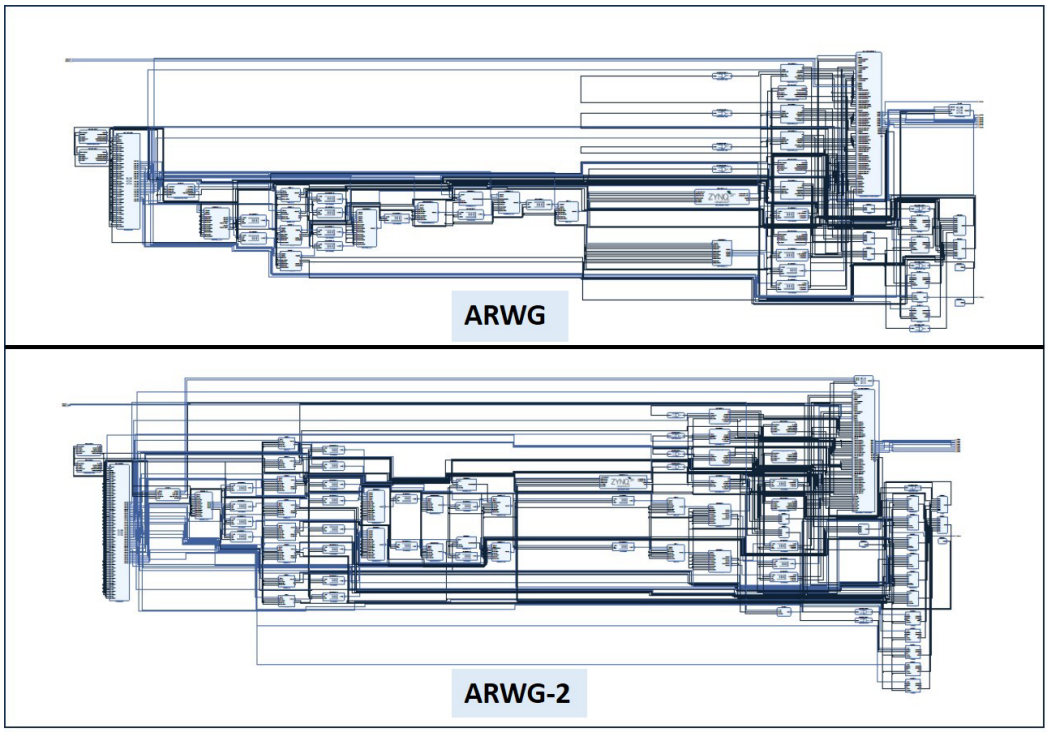

Figure 3. Comparison of block designs between ARWG and ARWG-2.

3. Interrupts

The key hardware innovation in ARWG-2 is interrupt handling. The Standalone CoreLink Generic Interrupt Controller (SCUGIC) on the Advanced Reduced Instruction Set Computer Machine (ARM) Cortex-A53 handles only 16 programmable-logic-to-processor-subsystem (PL-PS) interrupts natively. Xilinx provides an AXI interrupt controller (IntC) as an intellectual property (IP) block that is designed to allow up to 32 PL-PS interrupts per IP core, which can be further daisy-chained to service an arbitrary number of interrupts per processor. However, AXI IntC is not compatible with SCUGIC, that is, the designer can employ one but not both in the same processor.

A useful technique for developing RFSoC designs is to first prototype hardware–software design cores on the Zybo SoC, as the Zybo contains a very similar architecture (with exception of high-performance components such as the RF digital converter [RFDC]). After extended experimenting and prototyping AXI IntC designs on the Zybo, we were unable to realize a correct design. Therefore, the next best approach was to develop a custom IntC, which offloads some of the interrupt processing to IPs outside the processor. Our design is the forward interrupt controller (FIC). This relatively simple IP catches edge-sensitive interrupts provided by the ARWG signal generators, that is, the FM, BPSK, and variable DDS generators. These custom signal generators do not require any software acknowledgement, that is, the edge-sensitive interrupts are "fire-and-forget." Therefore, the AXI IntC is overly complex for our use case. The FIC catches edge-sensitive interrupts and sets a pending interrupt register, which is then passed to the SCUGIC to be serviced as a level-sensitive interrupt. Interrupts processed by FICs are independent; they can be asserted arbitrarily and in any order. The level-sensitive interrupt is asserted to the SCUGIC as long as any pending interrupts are present. The interrupt service routines, one per FIC, poll the pending interrupt status register to service the next highest priority interrupt. Upon servicing the interrupt, the pending interrupt bit in the FIC is reset.

Figure 4 shows the interrupt handling architecture in the ARWG-2 block design. In ARWG-2, 27 edge-sensitive interrupts are mapped onto 14 SCUGIC PL-PS interrupts (with two unassigned). The interrupts processed by FICs are the signal generator "lead" and "lag" interrupts, which are used for ARWG-2 techniques such as pulse group and frequency agility. Note that in SGUGIC Block 0 that four "VARDDSLOAD" interrupts map to one SCUGIC interrupt. These, however, are not processed by an FIC as they are codependent, meaning only one can be asserted at a time by definition. In Figure 4, the black interrupts are handled by SCUGIC as edge-sensitive and the red interrupts are handled as level-sensitive interrupts.

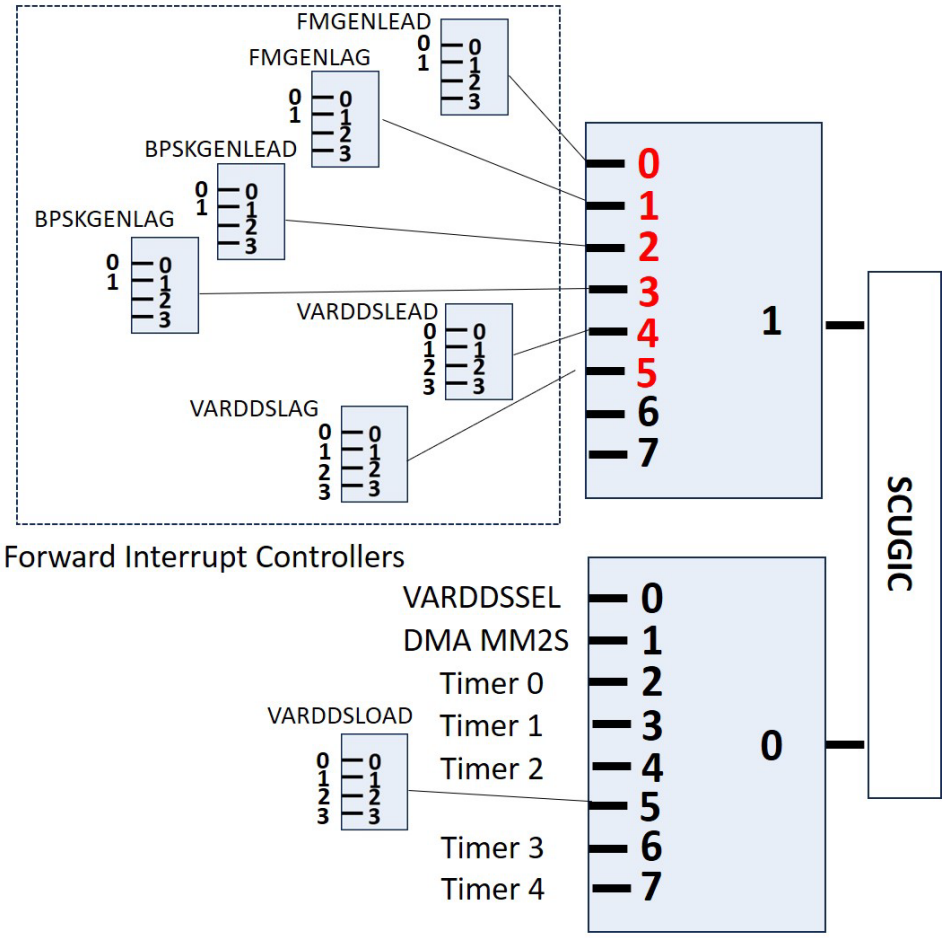

Figure 4. Taxonomy of interrupts and FICs in ARWG-2.

The FIC-defined interrupt architecture was prototyped on the low-cost Digilent Zybo board using user-defined and automated high-frequency interrupt sources consisting of AXI Timers. The prototyped design proved successful and therefore provided enough confidence to redesign the ARWG-2 hardware based on this architecture. The current interrupt architecture is robust enough to be scaled to an eventual four-channel architecture (e.g., ARWG-4).

4. Other Upgrades

The single-channel version of ARWG, which was itself inherited from earlier multichannel signal emulators, was well suited for expansion to ARWG-2. The key software change is to specify a channel context at the application level. The operator must always select a channel on which channel-specific operations are conducted. Additionally, any tabular arrays defined on signal generators are separated per generator and per channel. For example, if previously 16 FM waveforms could be defined and stored, the new number is 32 FM waveforms—16

per channel. Each channel has uniquely associated phase, amplitude, and noise modulators.

In addition to signal generators, the other main channel-specific upgrade is pulse group generation. Pulse groups and pulse group sequences are now defined on each channel. Since two AXI Timers are required to control pulse group sequences, two additional AXI Timers have been added to the hardware in ARWG-2. There are now a total of five AXI Timers in ARWG-2; one timer is held in reserve for future applications-layer control functions, for example, simulated dwell control from rotating antennas.

5. Results

Preliminary outputs of various multichannel scenarios are presented using the PicoScope 5000. Further verification of upgraded functions should be performed later using more capable test equipment such as Keysight oscilloscope and spectrum analyzers. Figures 5 and 6 show linear frequency modulation (LFM) radar pulses operated simultaneously in CH1 and CH2, where red and blue pulses represent differing channels. Figure 7 shows two simultaneous pulse trains with pulse groups and sequences of varying length and rest time.

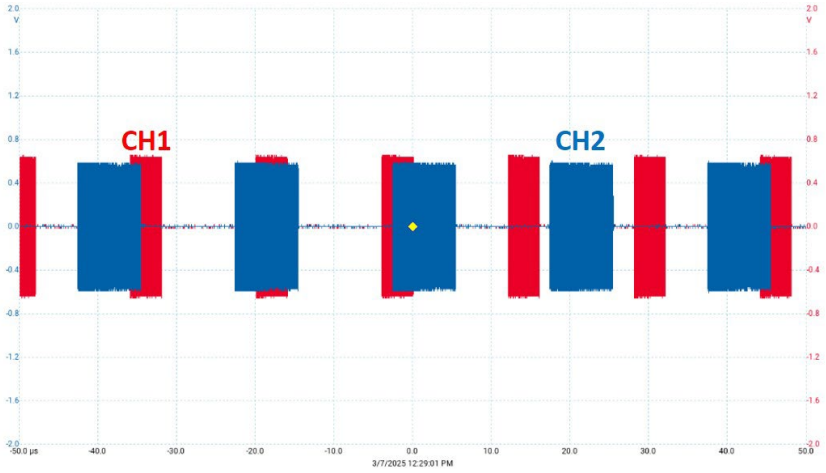

Figure 5. CH1 and CH2 LFM pulses in the time domain.

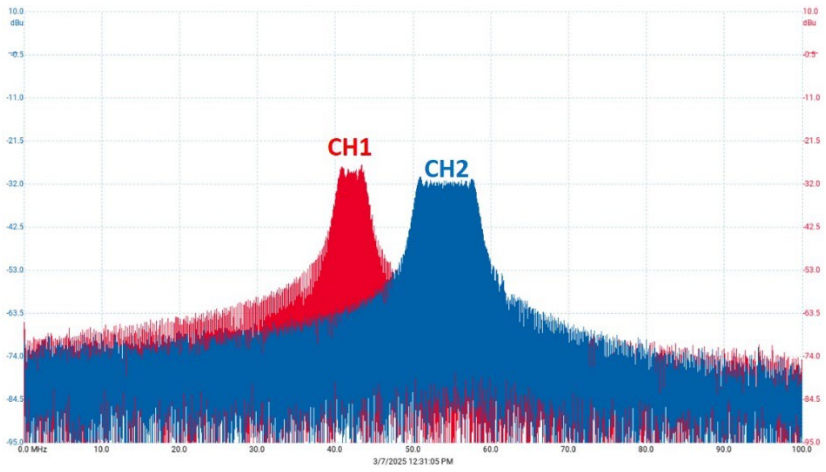

Figure 6. CH1 and CH2 LFM pulses in the frequency domain.

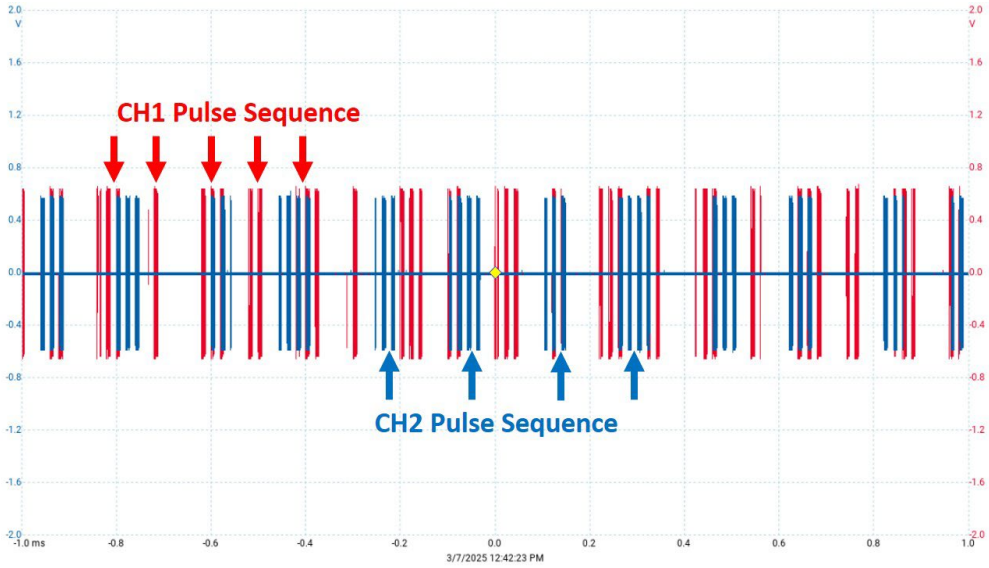

Figure 7. Simultaneous pulse group sequences on CH1 and CH2, respectively.

In addition to channels being independent, NCOs are completely independent, including selection of local frequency, Nyquist zone, and frequency agility parameters. In oscillator context, the user selects the desired oscillator at the application level, and all oscillation functions pertain to that oscillator. The NCO (0, 1, 2, or 3) is uniquely associated to a DAC Block (228, 229, 230, or 231) at hardware synthesis time. However, the exact output of each DAC block is configured by the user via external ports and baluns using the XM655 daughter card on the ZCU208. Figure 8 shows two simultaneous pulse-to-pulse frequency-hopping applications, with distinct numbers of channels, channel separation, and center frequency, on CH1 and CH2.

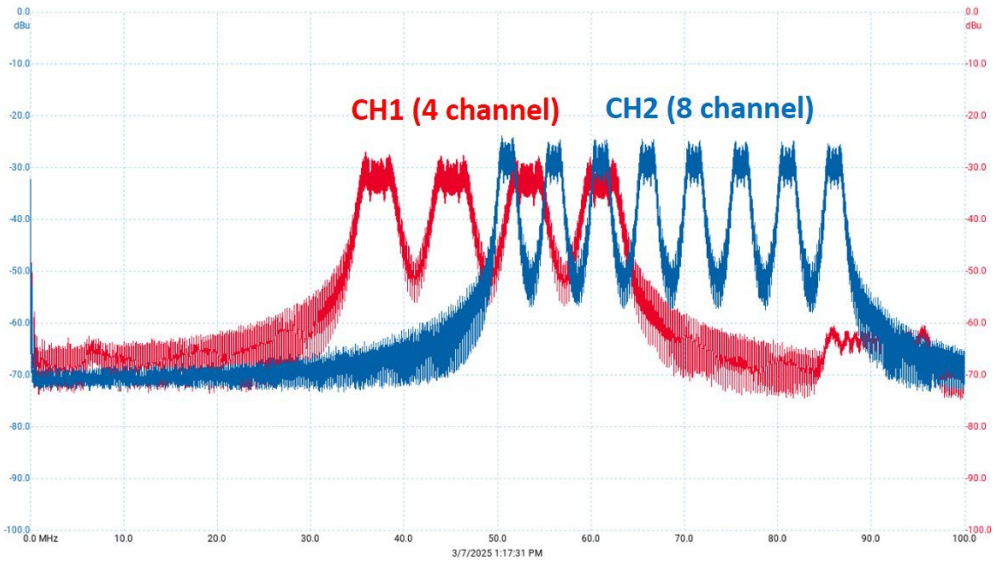

Figure 8. Two simultaneous LFM pulse trains with four frequency agility channels on CH1 and eight frequency agility channels on CH2, respectively.

6. Graphical User Interface

The ARWG-2 GUI has been updated to reflect the new functionality of two-channel ARWG and to enhance user experience. The green (online) and red (offline) channel icons at the bottom left of Figure 9 present the user-selected channel contexts. Upon toggling of channel context between CH1 and CH2, all tabular inputs stored in the GUI automatically toggle to reflect the correct context.

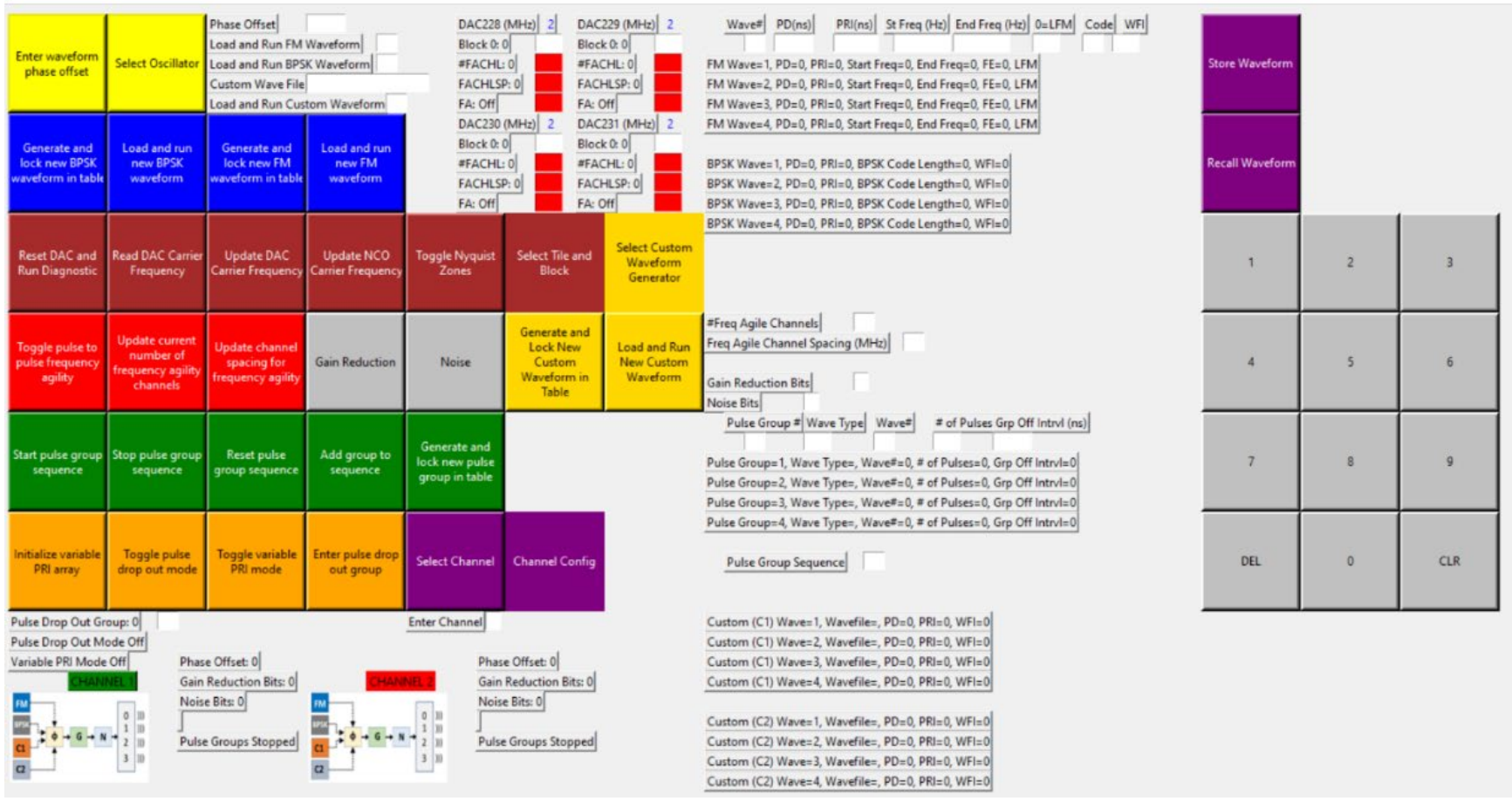

Figure 9. GUI upgraded for ARWG-2.

A numerical keypad implemented in **tkinter** interface has also been added to the GUI to allow touchscreen application. Finally, a store and recall function has been added to the FM waveform definition GUI to allow a user to store commonly used parameters and restore as necessary rather than retyping from scratch.

7. Implementation Statistics

Table 1 shows the hardware implementation statistics including a comparison of the baseline ARWG with ARWG-2. There were no changes in clocks between ARWG and ARWG-2. This turned out to be fortunate as clock redesign is manpower intensive. In terms of component utilization, memory- and arithmetic-centric channel components such as VARDDS and phase modulators essentially doubled with the addition of a second channel. In contrast, logic-centric components such as FM and BPSK generators caused less than a doubling of combinational logic components such as look-up tables (LUTs), registers, and slices. The updated ARWG-2 still only requires about 20% of the combinational logic resources of the FPGA, about 30% of the Block Random Access Memory (BRAM) resources, and a negligible percentage of the digital signal processor (DSP) resources. Utilization trends from ARWG to ARWG-2 show that the ZCU208 can easily support scaling up to four-channel ARWG, that is, ARWG-4, in the future.

Table 1. Implementation statistics for ARWG and ARWG-2 in Xilinx Gen3 RFSoC, including major parameters.

Clocks						
Component				This design MHz	Max MHz	
RFDAC Fs				3932.16	7000	
LMK04828				245.76	. . .	
LMX2594				491.52	. . .	
RFDC PLL ref				491.52	. . .	
AXI stream				245.76	. . .	
PL clock				100.00	. . .	
Utilization						
Component	**Available**	**ARWG**	**Percentage (%)**	**ARWG-2**	**Percentage (%)**	**Change (%)**
CLB LUT	425,280	31,676	7.45	53,085	12.48	67.59
CLB registers	850,560	21,942	2.58	31,204	3.67	42.21
CLB slice	53,160	7118	13.39	11,456	21.55	60.94
BRAM tiles	1080	157	14.54	309	28.61	96.82
BRAM32	1080	149	13.80	293	27.13	96.64
BRAM18	2160	16	0.74	32	1.48	100.00
DSP48E2	4272	17	0.40	34	0.80	100.00
Timing (ns)						
WNS		0.084		0.021		–75.00
Power (W)						
Total		8.020		8.372		4.39
RFDC		3.881		3.881		0.00
PS8		2.259		2.259		0.00
BRAM		0.195		0.386		97.95
Clocks		0.161		0.220		36.65

Notes: RFDAC = RF digital-to-analog converter; Fs = sampling frequency; RFDC = RF digital converter; PLL = phase-locked loop; AXI = Advanced eXtensible Interface; PL = programmable logic; ARWG = Advanced Radar Waveform Generator; CLB = combinational logic block; LUT = look-up table; BRAM = Block Random Access Memory; DSP = digital signal processor; WNS = worst negative slack; PS = processing system

Timing closure was achieved in ARWG-2, but barely, as there was a 75% decrease from worst negative slack (WNS) from 0.084 to 0.021 ns. It is unlikely that further logic additions can be made to the ARWG without requiring frequency replanning. By contrast, the power changes from ARWG to ARWG-2 were minimal. Total power is increased by only 4.39%, which is proportional to increased BRAM usage and more clock resources required for the second channel.

8. Conclusions and Future Work

We upgraded the ARWG from a single channel to a two-channel version called ARWG-2. This upgrade was completed in the field, namely, at the Chimera Forge Innovation Lab with the assistance of the 2MDTF in Mainz-Kastel, Germany. The combination of 2MDTF Soldiers and ARL technicians working together on this project is an innovative Army organizational construct that should be further explored. Future work could include scaling the ARWG design from two to four channels, porting this Xilinx Gen 3 RFSoC design into additional architectures, and incorporation of tailored hardware- and software-defined signal generation techniques.

9. References

1. Diehl W, Tesny N. Advanced radar waveform generator. DEVCOM Army Research Laboratory (US); 2023 Sep. Report No.: ARL-TR-9796.

List of Symbols, Abbreviations, and Acronyms

2MDTF	2nd Multi-Domain Task Force
AI	artificial intelligence
ARL	Army Research Laboratory
ARM	Advanced Reduced Instruction Set Computer Machine
ARWG-2	Advanced Radar Waveform Generator Two-Channel Upgrade
AXI	Advanced eXtensible Interface
balun	balanced to unbalanced
BPSK	binary phase shift key
BPSKGEN	binary phase-shift-keyed generator
BRAM	Block Random Access Memory
CH1	Channel 1
CH2	Channel 2
CLB	combinational logic block
DAC	digital-to-analog converter
DDS	direct digital synthesizer
DMA	direct memory access
DEVCOM	U.S. Army Combat Capabilities Development Command
DSP	digital signal processor
FIC	forward interrupt controller
FM	frequency modulation
FMGEN	frequency modulation generator
FPGA	field-programmable gate array
Fs	sampling frequency
Gen	generation; generator
GUI	graphical user interface
IntC	interrupt controller

IP	intellectual property
LFM	linear frequency modulation
LUT	look-up table
MHz	megahertz
ML	machine learning
NCO	numerically controlled oscillator
ns	nanosecond
PC	personal computer
PL	programmable logic
PL-PS	programmable-logic-to-processor-subsystem
PLL	phase-locked loop
PS	processor subsystem
RAM	Random Access Memory
RF	radio frequency
RFDAC	radio frequency digital-to-analog converter
RFDC	radio frequency digital converter
RFSoC	radio frequency system-on-chip
SCUGIC	Standalone CoreLink Generic Interrupt Controller
SoC	system-on-chip
VARDDS	variable direct digital synthesizer
WNS	worst negative slack

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