ARL-TR-10228 ● Nov 2025

Simulations of the Effects of Charge Traps in the Ferroelectric Hafnium-Oxide Gate Stack of Ferroelectric Field Effect Transistors (FeFETs) Under Pulsed Operation for Spiking Neural Networks

by Pankaj B. Shah

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14. ABSTRACT
Developing ferroelectric field effect transistors (FeFETs) for compute-in-memory and neuromorphic applications is a growing field of research. Technology computer-aided design drift-diffusion simulation results obtained at ARL for ferroelectric transistors and capacitors are presented in this report. Three leading commercially available software were considered for simulations to understand the status of commercially available software and determine where gaps exist. FeFET simulation results demonstrate how charge trapping would affect FeFET performance as a neuron or synaptic element in a spiking neural network.

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1. Introduction

The human brain has been the inspiration for neuromorphic computer systems because of the great advantages it possesses in operating power and volume (Najmaei et al. 2022). In the brain, neurons are nerve cells relaying information among different parts of the brain and to neurons throughout the body. Neurons communicate with other neurons by sending chemical and electrical signals in spikes (i.e., faster than 1 to over 400 ms) along synapses, which are paths chosen through experience. In neuromorphic computing, neurons and synapses are implemented through hardware. The advantage the brain has in operating power compared to today's computers has—in part—to do with how balancing energy consumption and information processing progressively evolved over millions of years. Neurons in the brain transmit information as action potentials (spikes) from neuron to neuron. These spikes consume energy; thus, there is a balance between spike firing rate and complexity of information being processed. An active area of research for meeting the challenges of neuromorphic computing is developing hardware using the advanced capabilities ferroelectric materials offer.

Ferroelectric materials are increasingly of interest for neuromorphic computing because of their demonstrated nonvolatile charge state and low power consumption, enabling neural and synaptic behavior along with non–von Neumann compute-in-memory architectures. Ferroelectrics are polycrystalline materials whose spontaneous polarization can be reversed with applied voltages. Hafnia ferroelectrics, such as thin-film hafnium oxide (HfO_2), hafnium-zirconium oxide (HZO), and doped variants (Si:HfO_2, Ce:HfO_2, Ir:HfO_2), can be integrated into the dielectric gate stack of a silicon MOSFET for use in neuron and synapse hardware of neuromorphic computers. The ferroelectric behavior is due to hafnium-oxygen bond distortion when in the orthorhombic crystal structure. Both synaptic and neural functions have been demonstrated with hafnia ferroelectric gated field effect transistors (FeFETs) (Luo et al. 2019, p. 122; Huo et al. 2024). For synaptic and compute-in-memory applications, the ferroelectric material is programmed into a charged state that capacitively modifies the conductance of the transistor conduction channel.

Ferroelectric HfO_2 and its variants are typically deposited by atomic layer deposition (ALD) followed by annealing. Ferroelectric properties emerge after annealing to crystallize it into metastable phases responsible for the ferroelectric behavior. The ALD process also creates an interfacial layer during material deposition; therefore, a high-quality SiO_2 layer is typically deposited to start, displacing the ferroelectric spontaneous polarization charge from the silicon surface. The polycrystalline HfO_2 gate dielectric contains many charge traps. Traps

are related to intrinsic point defects, such as oxygen vacancies, lattice disorders, and material interfaces. Both deposition processes (ALD, e-beam), postdeposition anneal step, or stresses in the device during operation can affect trap density. Also, processes to increase the dielectric constant or polarization properties, such as ion implantation, also affect the trap density (Zhang et al. 2025).

In ferroelectric devices charge traps are located at interfaces, in the bulk semiconductor, and dielectric and ferroelectric regions. These charge traps affect device performance with their charge, and the charge capture and release rates can greatly influence neuromorphic system performance. When used in spiking neural networks, the timing of pulses is important as it determines the energy used and the amount of information processed. Numerical simulations can help relate charge trap characteristics with the timing of signals applied to the FeFET during operation, showing trends that can help optimize FeFETs.

The goal of the activity discussed in this report is to develop an in-house capability at the U.S. Army Combat Capabilities Development Command (DEVCOM) Army Research Laboratory (ARL) to accurately simulate ferroelectric capacitors (FeCAPs) and transistors to guide development of these devices for next-generation neuromorphic electronics. Leading software are considered, key gaps are determined, and initial results are obtained for a sense of what directions are possible—to ensure that through communication with software vendors, the necessary simulation tools would be available to the research community. Having this simulation capability will speed neuromorphic circuit development because the compact model used for circuit design can be developed using trends obtained from technology computer-aided design (TCAD) simulations, rather than extracted from measured data that requires more fabrication time expenses.

2. Procedure

This work focuses on how TCAD can best be used to optimize ferroelectric devices for neuromorphic and compute-in-memory applications. This covers the following three areas: 1) finding appropriate and relevant device structures that can be simulated in commercial simulation packages, 2) evaluating scientific literature to determine key material concerns and related material parameters, and 3) seeing what commercial simulation software packages exist. Guidance for selecting the proper material models to optimize ferroelectric devices is also provided.

2.1 Devices to Consider

Two device structures of focus make use of these ferroelectric layers: FeCAP and FeFET. The FeCAP is a two-terminal charge-storage device consisting of ferroelectric and non-ferroelectric dielectrics between metal contacts. The FeFET considered here is a three-terminal voltage-controlled load-current device containing ferroelectric and non-ferroelectric dielectrics under the gate metal contact to capacitively control the drain-to-source current. To make use of the commercial state-of-the-art semiconductor ecosystem in the United States, the gate dielectrics of interest are those that can be integrated into the existing silicon fabrication lines at commercial fabrications (i.e., Intel, TSMC, and Samsung), either in front–end-of-line or back–end-of-line processes. In both structures, the ferroelectric material can be programmed to contain a nonvolatile charge state. Figure 1 shows a simulated FeCAP structure, and Figure 5 (left) shows the FeFET structure simulated in this work.

2.2 State-of-the-Art HfO_2 Quality

The HfO_2 gate dielectric in complementary metal-oxide–semiconductor technology has been developed since the early 2000s and was included in Intel and IBM commercial production beginning in 2007 because it allows for a physically thicker gate dielectric layer, which is needed for low leakage currents as the devices scale to shorter gate lengths. Trap densities in HfO_2 on silicon are much higher than those in SiO_2 on silicon. Doping HfO_2 for use as ferroelectric gates may increase the amount of charge trapping observed. Also, HfO_2 has been used in resistive random access memory where oxygen vacancies form conductive filaments whose formation and rupture lead to low- and high-resistance phases, indicating the propensity of charge traps to form as the oxide-layer crystallinity changes during operation under electrical stresses.

The literature on HfO_2 provides valuable information and shows that at this stage material quality (i.e., charge trap density) varies widely. Considering bulk traps, Salomone et al. (2025), fit pulsed capacitance-voltage data for an ALD HfO_2 on silicon structure and obtained a trap density of 1.2×10^{21} cm^{-3}, a trap energy level of 1.12 eV, and a carrier lifetime of 5 ns. The estimated SiO_2 layer thickness between HfO_2 and silicon may be up to 3 nm thick (Salomone et al. 2025). Zhou et al. (2023) used pulsed polarization measurements on a doped HfO_2/SiO_2/silicon ferroelectric transistor gate stack and compared results to Landau–Ginzburg simulations, obtaining a trap density of 4×10^{20} cm^{-3} in the HfO_2 layer at energy levels of 2.9 and 1.7 eV below the conduction band edge. O'Sullivan et al. (2020), obtained from a Si: HfO_2/SiO_2 gate dielectric stack FeFET threshold–voltage–shift

measurements, a bulk trap density of 5×10^{19} cm^{-3} in the ferroelectric layer, at an energy level of 0.33 ± 0.1 eV below the conduction band. Finally, Kim et al. (2025), obtained an electron trap density of 5×10^{20} cm^{-3} and a hole trap density of 5×10^{19} cm^{-3} in HfO_2 from Vth shift measurements.

Regarding interface trap densities at the HfO_2/SiO_2 interface, Toprasertpong et al. (2022) discusses a trap density of 1×10^{14} cm^{-2} comparing quasistatic split capacitance voltage and gated hall measurements. Bersuker et al. (2007), fit drain current transient data for a HfO_2/SiO_2 gate stack field effect transistor (FET) to obtain an interface trap density of 1×10^{14} cm^{-2}. Zhang et al. (2014), measured from memory window shifts of an $Au/HfO_2/SiO_2/Si$ structure a donor type trap density of 4×10^{12} cm^{-2}. Meihar et al. (2024), obtained from simulations of memory window shifts an interface trap density of 2.7×10^{12} cm^{-2}. Also, Higashi et al. (2021), obtained a trap density of 1.3×10^{13} cm^{-2} from memory window measurements on a $TiN/HfO_2/SiO_2/Si$ stack.

Charge pump measurements also give varying trap density results. Woo et al. (2023), obtained an interface trap density between 0.64 and 1.37×10^{11} cm^{-2}/eV for HSO and between 0.11 and 0.49×10^{11} cm^{-2}/eV for HZO. An et al. (2025), measured for a HZO-based MFMIS structure a trap density of 1×10^{16} cm^{-3}/eV. Also, an interface trap density of 4.2×10^{10} cm^{-2}/eV was obtained from charge pump measurements.

2.3 TCAD Modeling Software and Included Models

TCAD involves using a 2D or 3D model of a device to obtain the external currents resulting from applied voltages, or external voltages determined from applied currents to a semiconductor device that includes metal contacts and insulator regions. Also, charge-carrier and electrostatic-potential distributions can be visualized. Valuable results are obtained using relevant and accurate material physics models. The equations of interest are the charge-carrier continuity equation and Poisson's equation. These equations are numerically solved over a mesh covering the 2D device structure. Obtaining a solution can be challenging because the equations are ill-conditioned, making the solution sensitive to very small changes in the data. These small changes are related to the large exponential variation in charge-carrier concentration across the device structure, disparate physical scales, and the nonlinear coupled equations.

To save time, a commercial simulation package with physics-based models is desired. The models would be fit to match measured material characteristics. For TCAD, three software packages are under consideration: Silvaco Group, Inc., has developed the software Victory Device (referred to here as Silvaco); COMSOL AB

has developed COMSOL Multiphysics (referred to here as COMSOL); and Synopsys, Inc., has developed Sentaurus Device (referred to as Sentaurus). Each software has advantages and disadvantages, which will be discussed below. With access to COMSOL and Silvaco software, more information could be obtained as provided here than for Sentaurus and only simulation results obtained from Silvaco are presented.

Both Silvaco and Sentaurus are focused on semiconductor electronics and take input in a text-based format. COMSOL is a multiphysics software used in many different fields besides semiconductor devices, and its input is fully GUI-based. Text-based visibility of all models in one file is helpful for error checking and debugging.

The spontaneous polarization of ferroelectric dielectrics plays an important role in ferroelectric device performance and analysis. This polarization state is set by applying a voltage across the dielectric layer. Then, subsequent voltages applied to the device (i.e., gate voltage of a FeFET) may or may not add to the spontaneous polarization in a ferroelectric region depending on the range of the newly applied voltage by flipping domains that were not flipped by previously applied voltages. The ferroelectric models currently available in COMSOL or Silvaco could not do this. In these software packages, when the voltage across the ferroelectric material is reversed, the spontaneous polarizations of previous voltages are not remembered. There is no history of a previous spontaneous polarization charge in their models. Sentaurus will also be investigated for this capability, although the manual mentions that polarization turning points are memorized (Synopsys 2024). This type of simulation is important when simulating imprint measurements on ferroelectric capacitors and depolarization effects related to retention and endurance of a FeFET (Vecchi et al. 2025).

As discussed earlier, charge trapping in the ferroelectric layer is very important to include in the ferroelectric device model; however, both Silvaco and COMSOL do not have charge trapping models that work for bulk dielectrics or the interface between two dielectrics. COMSOL has a new electrostatic discharge module that can model charge trapping in oxides, but it is not currently available with ARL's in-house purchased software. For this report, the FeFET ferroelectric dielectric is simulated as a semiconductor with appropriate material parameters so that bulk dielectric traps can be included in the ferroelectric-HfO_2 region, and interface traps are included at the interface between HfO_2 and SiO_2. The spontaneous polarization charge of the ferroelectric region is set using an interface charge model, rather than the built-in ferroelectric polarization models. Fowler–Nordheim tunneling models the charge leakage through the SiO_2 layer of the FeFET. The FeFET silicon layer

charge-carrier mobility is modeled considering doping, inversion layer effects, and remote coulomb scattering.

3. Results

3.1 FeCAP

The FeCAP (Figure 1) contains a ferroelectric HfO_2 layer on a silicon layer all sandwiched between electrical contacts. The Empirical Ferroelectric polarization model in Silvaco that relates ferroelectric spontaneous polarization charge to applied voltage is used for the results presented in this section but only works on insulator layers. To see the effects of the ferroelectric polarization charge one needs to add a silicon layer to force the program to calculate the charge carriers present in response to the applied voltages and the ferroelectric spontaneous polarization. This then causes the program to calculate the free-carrier density in the semiconductor region adjacent to the ferroelectric dielectric layer. The donor density of the silicon layer was set to 1×10^{20} cm^{-3} to mimic the high free-electron charge density at the semiconductor–insulator interface of a FET structure with only body and gate contacts. TCAD of FeCAPs is a quick way to see how polarization changes with layer thicknesses as well as effects of changing non-ferroelectric layers in the gate stack, such as the distribution of potential in the material stack. Unfortunately, the software does not allow traps in the dielectric bulk or at interfaces between two bulk dielectrics; thus, effects of charging traps in the HfO_2 region are not simulated in this section.

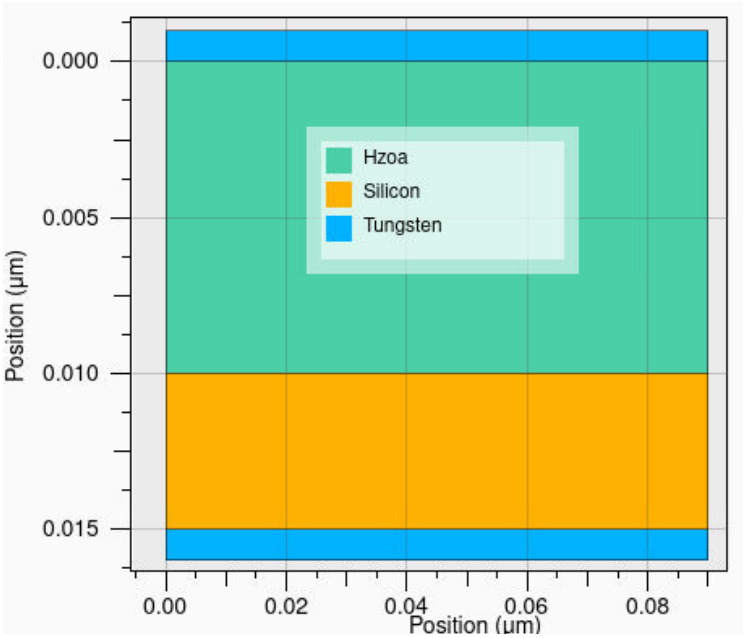

Figure 1. 2D cross section of the FeCAP simulated.

Figure 2 shows one-half of the polarization versus voltage hysteresis curve matching typical ferroelectric HfO_2 measured data. The empirical ferroelectric model in Silvaco had parameters set as follows: Ferro.pr = 28×10^{-6} C/cm^2, ferro.ps = 31×10^{-6} C/cm^2, ferro.ec = 0.9×10^6 V/cm, ferro.epsf = 60, permittivity = 60.

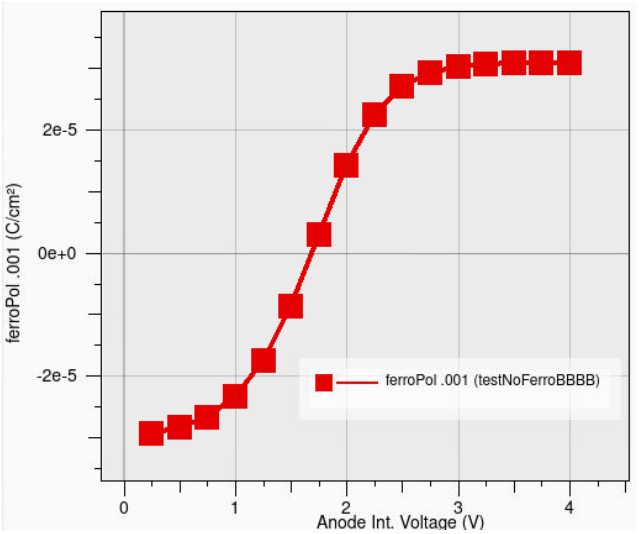

Figure 2. Right half of a polarization–voltage hysteresis curve for a typical ferroelectric HfO_2 capacitor.

The free-electron density is increased in the silicon layer near the ferroelectric dielectric due to the presence of the modeled ferroelectric region charge (Figure 3), showing the peak value near 0.01 µm. Here, we see that the free-electron concentration increases along a vertical cutline from (x, y) = (0.04 µm, 0.01 µm) to (0.04 µm, 0.015 µm) of Figure 1, when the ferroelectric polarization model is included (red) compared to the case without it—in which case, the electron concentration is determined only by the applied voltage across the device and the potential barrier due to discontinuous conduction band.

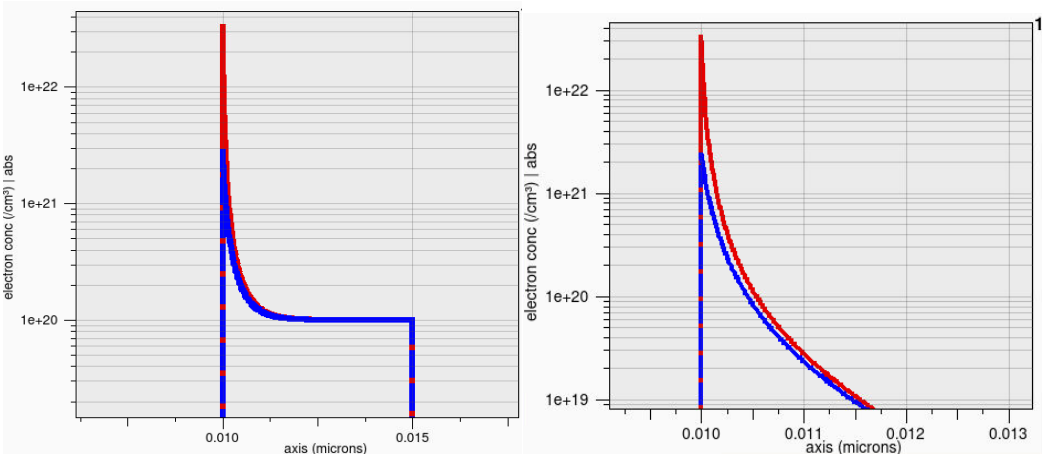

Figure 3. Plots showing V = 3V carrier concentration at interface between semiconductor and dielectric, demonstrating increased carrier concentration when polarization model is present.

Band bending and electrostatic potential distributions are shown in Figure 4.

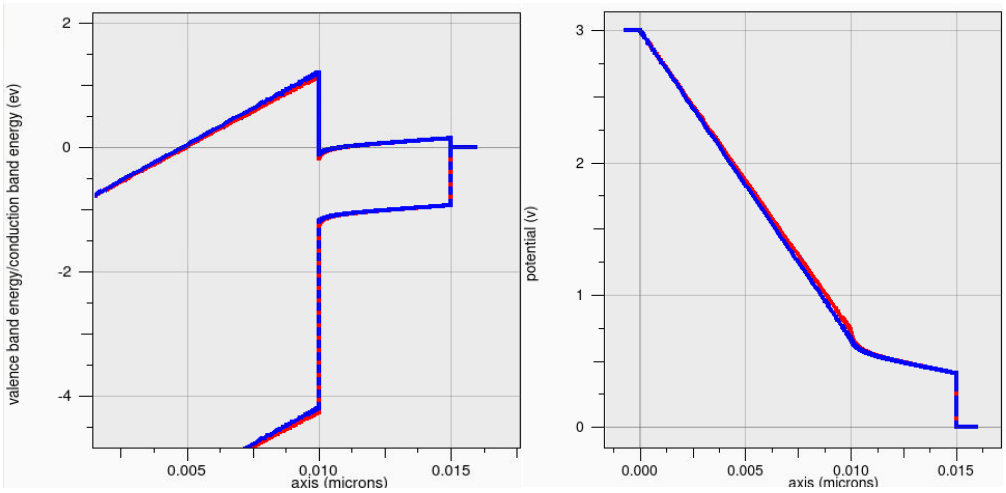

Figure 4. HfO_2/silicon (left) energy band structure and (right) potential distribution from top electrical contact to bottom contact for simulations with (red) and without (blue) the empirical ferroelectric model.

3.2 Transient Analysis of FeFET

The FeFET device being simulated here is considered preprogrammed with a ferroelectric charge (weight) as would occur when implemented in a crossbar array implementation of a neuromorphic circuit synapse to see how it reacts to spiking voltages. Simulations similar to these can help optimize the gate dielectric layer stack for proper timing, improve the memory window, and increase endurance as will be discussed. Models included in the results shown are charge trapping in the ferroelectric HfO_2 region and the HfO_2/SiO_2 interface; Fowler–Nordheim tunneling through the SiO_2 layer; and electron mobility accounting for doping, inversion layer effects, and remote coulomb scattering.

The device structure analyzed as a FeFET is shown in Figure 5 (left) and the donor density of the silicon region is shown in Figure 5 (right). The red regions in the upper left and right of Figure 5 (right) are high doped, as is typically done to form good source and drain electrical contacts to the silicon region and to be a large reservoir of mobile electrons in the channel.

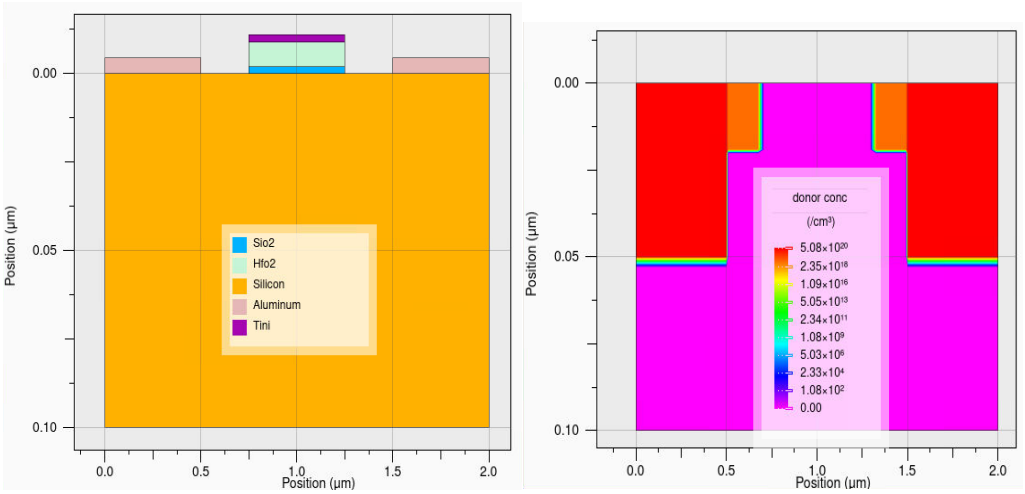

Figure 5. (Left) 2D cross section of the FeFET structure simulated. (Right) Donor concentration in the silicon region. The background acceptor concentration of 5×10^{15} cm^{-3} throughout the silicon region is not displayed. The SiO_2 interlayer region is 2 nm thick and the HfO_2 region is 7 nm thick.

In these simulations, we assume that the ferroelectric material is programmed into a set charge state. This charge would be equivalent to the desired weighting of the FeFET in the crossbar array type of synapse circuit element of a spiking neural network. As discussed in the literature, the ferroelectric layer's spontaneous polarization charge in a real ferroelectric FET is much lower than that obtained from polarization-voltage measurements on a capacitor of the same dielectric material (Nigon 2017, p. 71; Si et al. 2021; Toprasertpong et al. 2022). The difference is due to depolarization fields in the silicon layer, charge trapping, leakage currents and fabrication-related material variability, and material relaxation due to crystallinity changes.

Therefore, to determine what fixed ferroelectric spontaneous polarization charge to use (as the weight), Vgs = 2V and Vds = 0.2 V are simultaneously applied to it and the resulting channel electron density along a vertical cutline in the silicon region under the gate is integrated for different ferroelectric spontaneous polarization charges at the ferroelectric HfO_2/SiO_2 interface to determine which ferroelectric layer charge leads to a desired on-state electron density in the channel. Figure 6 (left) shows the electric field and Figure 6 (right) shows the band structure for ferroelectric charge densities of 9×10^{13} cm^{-2}, $7e \times 10^{13}$ cm^{-2}, 5×10^{13} cm^{-2}, and 3×10^{13} cm^{-2}, placed at the interface between the ferro-HfO_2 and the SiO_2.

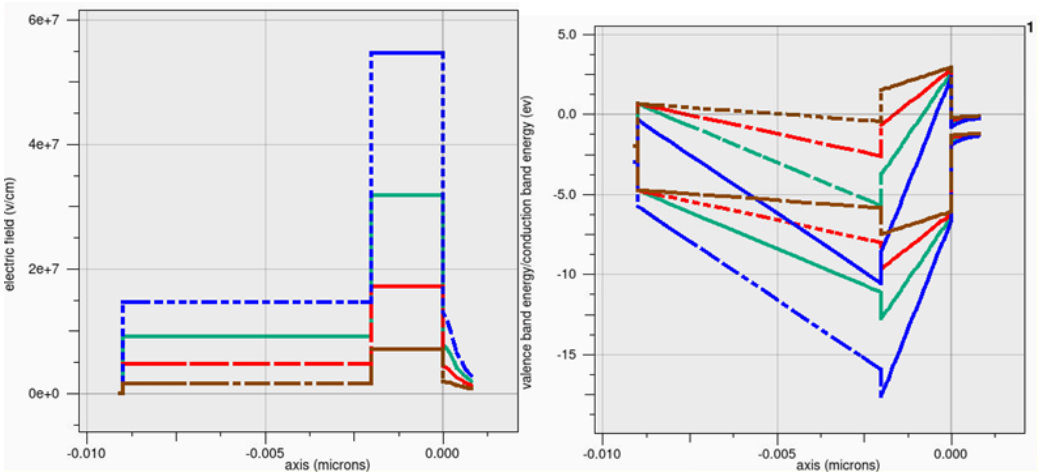

Figure 6. (Left) Electrostatic field across the oxide stack for a vertical cutline through the HfO_2/SiO_2/silicon stack (shown in Figure 5 [left]) for ferroelectric layer spontaneous polarization charges of 9×10^{13} cm^{-2} (blue), 7×10^{13} cm^{-2} (green), 5×10^{13} cm^{-2} (red), and 3×10^{13} cm^{-2} (brown). SiO_2 is 2 nm and HfO_2 is 7 nm thick. Vgs = 2 V, Vds = 0.2 V, for the first three curves, and Vgs = 3 V, Vds = 0.2 V, for the blue plot due to convergence issues. (Right) Corresponding energy band diagrams showing conduction and valence bands.

The free-electron density in the silicon channel is 1.48×10^{14} cm^{-2}, 8.45×10^{13} cm^{-2}, 4.46×10^{13} cm^{-2}, and 1.79×10^{13} cm^{-2}, which is obtained by integrating the electron concentration plot shown in Figure 7. This last concentration value is close to the maximum expected, thus the ferroelectric layer's spontaneous polarization was set to a fixed interface charge of 3×10^{13} cm^{-2}. A ferroelectric surface charge of 3×10^{13} cm^{-2} is equivalent to a polarization charge of 4.8 uC/cm^2 ($P/1.6 \times 10^{-19}$ = density), which is close to the value measured by Dahan et al. (2025) for a Global Foundries FeFET. Another item to note is that (as seen in Figure 6 [left]) for sheet charge density above 3×10^{13} cm^{-2}, the field across the SiO_2 layer is larger than the SiO_2 breakdown voltage of 10 MV/cm.

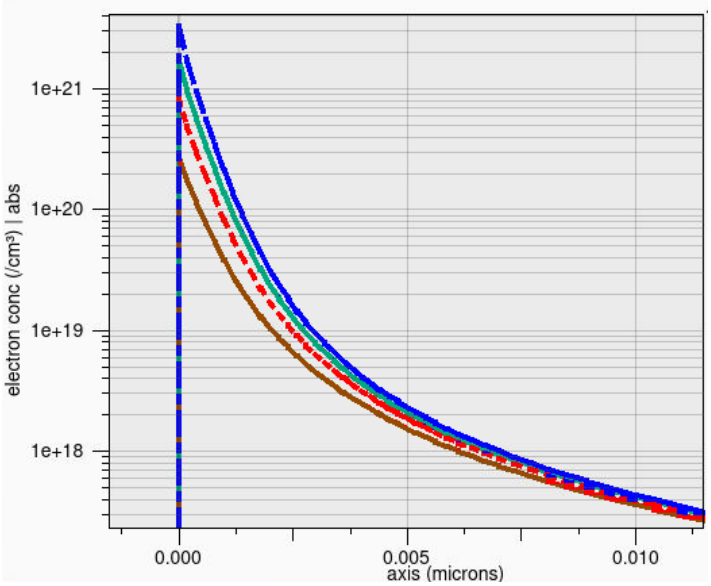

Figure 7. Calculated electron concentration vs. depth in the channel of the FeFET for ferroelectric HfO_2 polarization charges of 9×10^{13} cm^{-2} (blue), 7×10^{13} cm^{-2} (green), 5×10^{13} cm^{-2} (red), and 3×10^{13} cm^{-2} (brown). The Vgs = 2V, Vds = 0.2V, for the first three curves, and Vgs = 3V, Vds = 0.2V, for the blue plot due to convergence issues.

As the ferroelectric region charge density stepped down from 3×10^{13} cm^{-2} to -2×10^{13} cm^{-2} the transfer characteristics shifted to higher voltages (Figure 8). In all cases the bulk charge trap density in the ferroelectric layer is set to 9×10^{17} cm^{-3}.

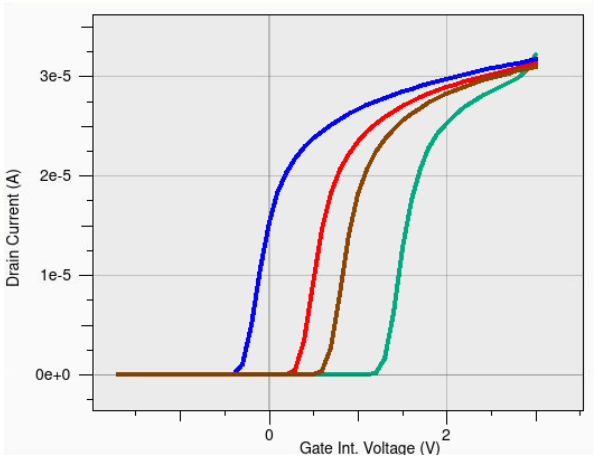

Figure 8. Plot showing the movement of the threshold voltage as the ferroelectric charge decreased from left to right: 3×10^{13} cm^{-2} (blue), 1×10^{13} cm^{-2} (red), -1×10^{13} cm^{-2} (brown), and -2×10^{13} cm^{-2} (green).

The bulk charge trap density in the HfO_2 also shifts the threshold voltage (Figure 9). There, the threshold voltage shifts right as the trap density in the ferroelectric HfO_2 layer increases from a low value of 9×10^{17} cm^{-3} (green) to 4×10^{20} cm^{-3} (red). This higher value along with the trap acceptor energy level of 1.7 eV (below conduction band and donor energy level of 2.5 eV above valence band)

were chosen to match the trap characteristics measured by Zhou et al. (2023). The threshold voltage determines the memory window voltage extent, affects the number of synaptic weights that can be represented with higher precision, and influences both circuit compatibility with external elements and tolerance to device variations.

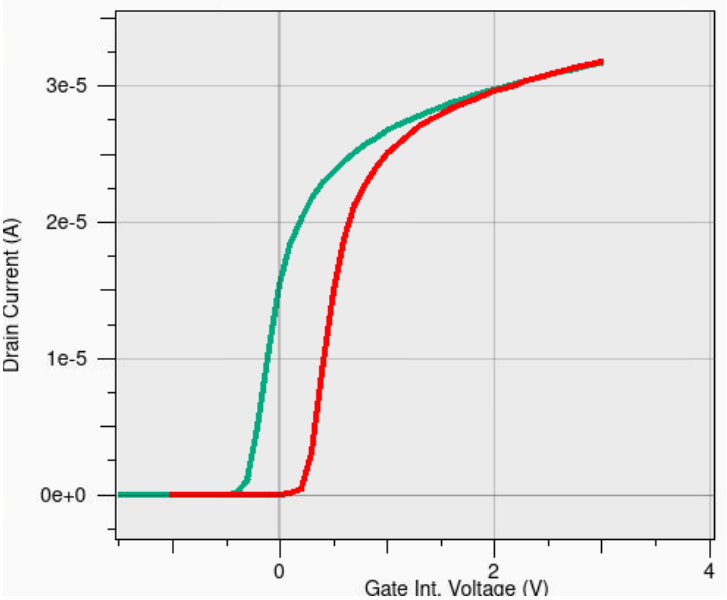

Figure 9. Transfer characteristic showing the threshold voltage for ferroelectric HfO_2 trap densities of 9×10^{17} cm^{-3} (green) and 4×10^{20} cm^{-3} (red).

With the ferroelectric HfO_2 charge fixed to 3×10^{13} cm^{-2}, spiking operation of the FeFET was simulated by fixing one of the applied voltages and pulsing the other to see the effect of charge trapping on spiking operation of the synaptic or neuron element. First, the drain voltage is fixed and the gate voltage is pulsed (as shown by the black dashed line in Figure 10). The rise time can be adjusted but is taken here as 2 µs. The high-level duration is 1 µs and the fall time is also 2 µs. As the bulk trap density in the ferroelectric HfO_2 region increases, the drain current overshoot increases, and pulse width decreases (as seen with the blue curve compared to the red and green curves in Figure 10).

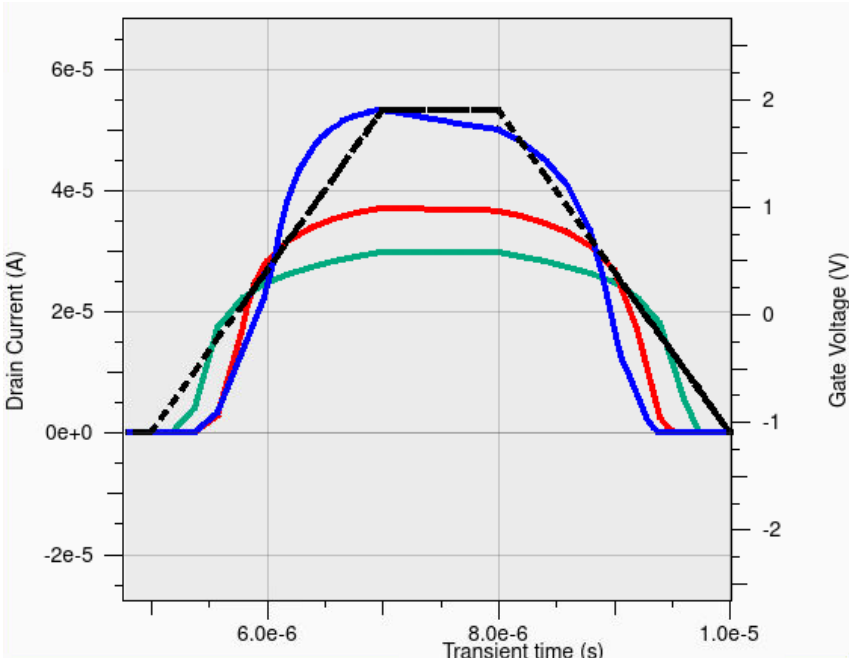

Figure 10. FeFET simulation results showing the resulting drain current pulse for ferroelectric HfO_2 in the gate stack with a trap density of 4×10^{20} cm^{-3} (blue), 1×10^{20} cm^{-3} (red), and 4×10^{18} cm^{-3} (green). The applied gate voltage pulse is shown in black and Vds = 0.2 V.

Of the key parameters of a charge trap, it was observed in these simulations that varying the trap density in the ferroelectric HfO_2 region had a great influence on changing device performance compared to changing the trap energy level or cross section.

Conversely, if the gate voltage is fixed and the drain voltage pulsed, simulations indicate that the transient profile of the drain current signal is wider than the drain voltage pulse and increases as the trap density in the ferroelectric HfO_2 layer increases (Figure 11).

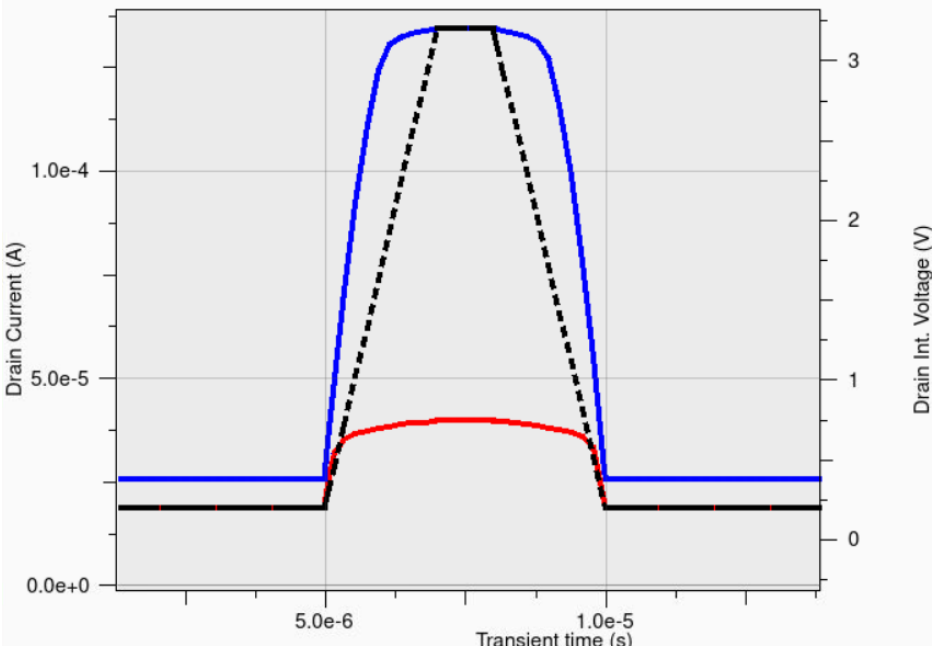

Figure 11. Drain current for spiking drain voltage. Bulk trap density of 4×10^{20} cm^{-3} (red) and 4×10^{18} cm^{-3} (blue). The Vgs = 0.6 V. The drain voltage pulse is shown dashed in black.

4. Conclusions

Numerical simulations of ferroelectric FETs are a valuable research technique to both understand measured results and optimize the performance of FeFETs for spiking neuromorphic applications. The simulations can help improve the timing of the synaptic elements, as well as adjust the memory window. Seeing how varying the charge traps in different regions of the gate dielectric can affect device performance gives another knob to control for FeFET optimization. This work also identified software gaps that need attention as the industry moves toward compute-in-memory and neuromorphic applications. The next step is to communicate with the software vendors to add items of interest to the compute-in-memory and neuromorphic computing research community.

5. References

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List of Symbols, Abbreviations, and Acronyms

2/3D	two-/three-dimensional
ALD	atomic layer deposition
ARL	Army Research Laboratory
DEVCOM	U.S. Amry Combat Capabilities Development Command
FeCAP	ferroelectric capacitor
FET	field effect transistor
FeFET	ferroelectric gated field effect transistor
GUI	graphical user interface
HfO_2	hafnium oxide
HZO	hafnium-zirconium oxide
TCAD	technology computer-aided design

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