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DEVCOM ARMY RESEARCH LABORATORY

Radio Frequency (RF) Interface Concept Development for the Defense Advanced Research Projects Agency (DARPA) Digital RF Battlespace Emulator Program

by Ed Viveiros, Daniel Galanos, and William Diehl

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Radio Frequency (RF) Interface Concept Development for the Defense Advanced Research Projects Agency (DARPA) Digital RF Battlespace Emulator Program

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The US Army Combat Capabilities Development Command Army Research Laboratory has completed a study on RF interface requirements in support of the Defense Advanced Research Projects Agency's Digital RF Battlespace Emulator (DRBE) program. This study was completed under Phase I of the DRBE program in collaboration with the Massachusetts Institute of Technology–Lincoln Laboratory, which has primary responsibility for system integration. The goal of the study is to determine the requirements for an RF interface capable of supporting 80–200 systems under test in the emulator environment. Follow-on phases of the program will lead to full-scale development of the DRBE system.

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1. Introduction

The US Army Combat Capabilities Development Command Army Research Laboratory has completed a study on RF interface requirements in support of the Defense Advanced Research Projects Agency (DARPA) Digital RF Battlespace Emulator (DRBE) program.[1] This study was completed under Phase I of the DRBE program in collaboration with the Massachusetts Institute of Technology–Lincoln Laboratory (MIT-LL), which has primary responsibility for system integration. The goal of the study is to determine the requirements for a RF interface capable of supporting 80–200 systems under test (SUTs) in the emulator environment. Follow-on phases of the program will lead to full-scale development of the DRBE system.

The primary function of the RF interface is to provide interconnections between the analog SUTs and the digital real-time high-performance computer (RT-HPC). The RF interface will provide analog signal conditioning, analog-to-digital/digital-to-analog conversion (ADC)/(DAC) and digital control interface for the SUTs and the RT-HPC. The digital control interface will exchange information with the RT-HPC via an application programming interface (API).

2. DRBE Background

The goal of the DRBE program is to create a large-scale virtual RF test range capable of emulating a realistic, complex, RF signal environment. The DRBE concept, shown in Fig. 1, will support development, testing, and training of advanced cognitive radar and electronic warfare (EW) systems. The primary effort under the program is development of an RT-HPC with high computational capacity and extremely low latency, enabling numerous RF systems to interact in a virtual environment.

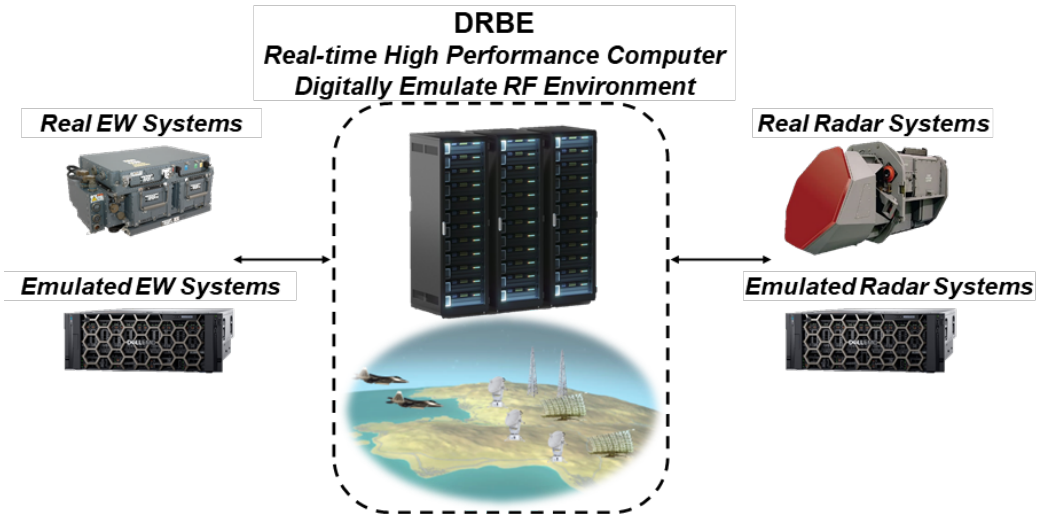


Fig. 1 DRBE concept

The DRBE RT-HPC will interface to an array of real and emulated EW, radar, and SUTs, allowing a variety of scenarios to be emulated on a virtual battlefield. The DRBE program is also pursuing a system integration effort to develop and provide the necessary tools and hardware for complete implementation of the virtual environment, including scenario generation, physical interfaces between the SUTs and RT-HPC, API, and reference algorithms. Development of general-purpose digital RF emulators is planned for future phases of the program.

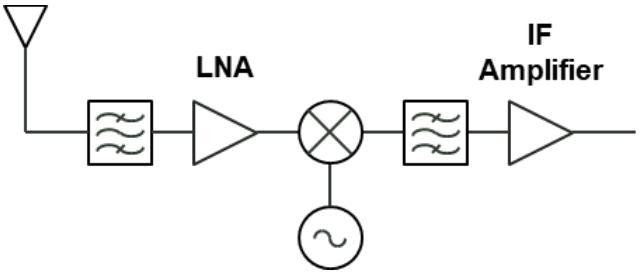
DRBE system-level metrics relevant to the RF interface development are shown in Table 1. The minimum latency metric may be challenging to meet in the RF interface. The DRBE Broad Agency Announcement (BAA) specifies a minimum total latency of 3.3 μs with a maximum of 2.5-μs latency allocated to the RT-HPC, leaving only 800-ns latency through the RF interface. This 800-ns latency must be split between the transmit (Tx) and receive (Rx) interfaces since all DRBE scenarios involve interactions between Tx and Rx SUTs. Current commercial off-the-shelf (COTS) data converters should be capable of meeting the average Tx/Rx instantaneous bandwidth (IBW). Frequency coverage was not defined as a metric for the program, though the BAA describes systems operating over a band from near 0 to well over 10 GHz. Additional DRBE program details can be found in the BAA.[1]

Table 1 DRBE system-level metrics

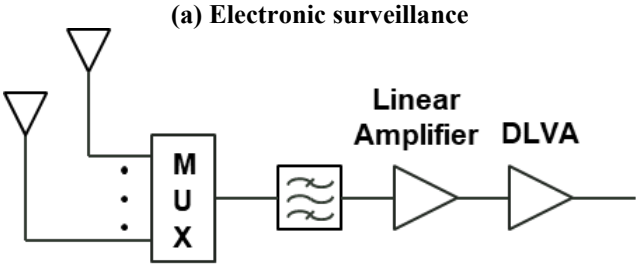
Metric	Threshold	Objective
Number of total systems	80	200
Minimum latency / range	3.3 μs / 1 km	3.3 μs / 1 km
Maximum latency / range	3300 μs / 2 × 500 km	3300 μs / 2 × 500 km
Average Tx IBW	1 GHz	1 GHz
Average Rx IBW	2 GHz	2 GHz
Environment update rate	100 Hz	1 kHz

3. RF Interface Design Considerations

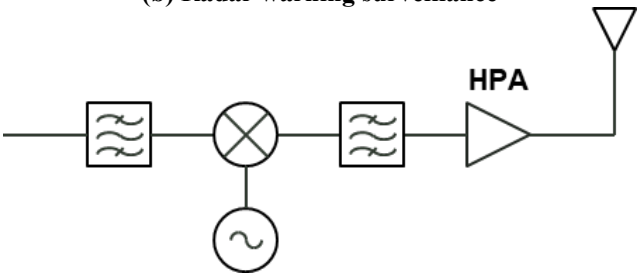
DRBE should be capable of interfacing with a wide variety of SUT classes including Rx-only, Tx-only, and Tx/Rx. Sample notional SUT block diagrams for the different classes, as shown in Figs. 2a–e, include electronic surveillance and radar warning receivers, electronic attack (EA)/jammer transmitter, radar, and digital RF memory (DRFM). Receivers typically include a low-noise amplifier (LNA) in the front-end to set the lower end of the receiver dynamic range. Some receivers include a limiter prior to the LNA to protect it from damage due to high power from interference or jammer signals. Transmitters typically have a high-power amplifier (HPA) as the last stage prior to the antenna. Typical HPAs include vacuum tubes, such as a travelling wave tube amplifier (TWTA), or solid-state electronic devices, such as gallium arsenide or gallium nitride. Modern RF systems typically use DACs to generate baseband waveforms and ADCs to capture received signals for digital postprocessing.



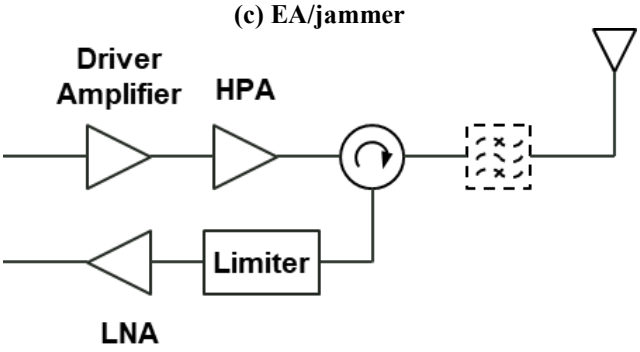
(a) Electronic surveillance



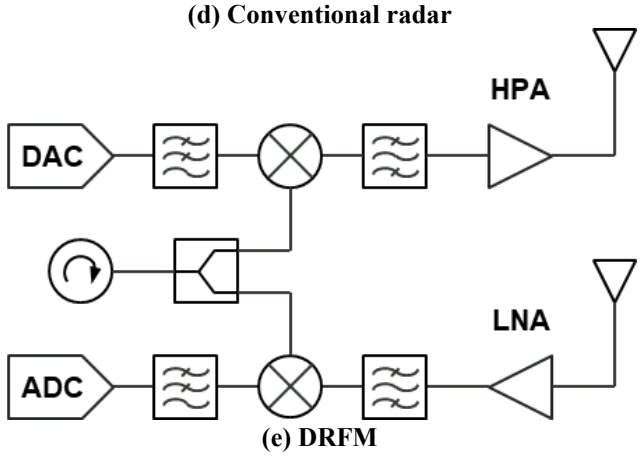
(b) Radar warning surveillance



(c) EA/jammer



(d) Conventional radar

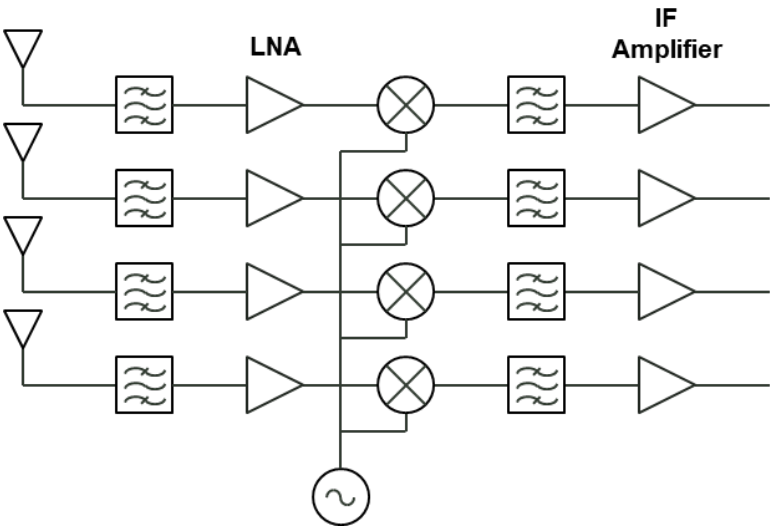


(e) DRFM

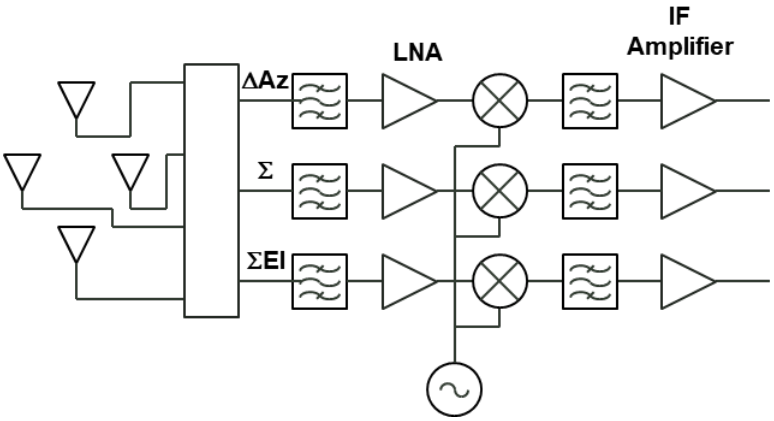
Fig. 2 Notional SUT class block diagrams

It is not expected that SUTs will transmit and receive radiated signals with their antennas, as this would require a large anechoic chamber capable of handling very-high-power levels because the SUTs could be capable of transmitting kilowatts of power. The RF interface should connect to the SUT as close to the antenna as possible for signal extraction/injection to maintain fidelity of the SUT signals. In cases where additional components in the SUT must be bypassed, such as the power amplifier (PA), the characteristic response of those components must be applied to the signals to ensure accurate representation. Each SUT will need to be studied in detail to identify the optimal connection point for DRBE interface and what additional signals and/or information is needed, such as frequency, IBW, Tx power, antenna pattern, and beam steering commands, to accurately emulate the SUT.

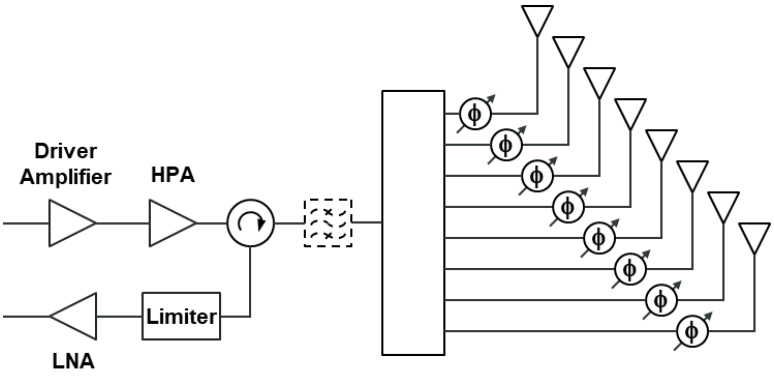
DRBE should also be capable of interfacing with a variety of multiport SUTs (examples shown in Figs. 3a–d), such as direction finding (DF) and monopulse receivers and passive/active array radars. DF and monopulse systems can use either amplitude or phase comparison to measure angle of arrival of the received signal. Passive array radar transmitters are typically driven by an HPA and implement phase shifters at the antenna elements to enable beam steering. Active array radars distribute Tx/Rx modules at the antenna elements that include LNAs, PAs, and phase shifters for beam steering. The RF interface should be capable of interfacing to multiport SUTs using a minimum number of DRBE RT-HPC ports that might require implementation of port-reduction techniques. Multiport SUTs that are not amenable to port reduction, such as large phased arrays, may require multiple RT-HPC ports for operation within the DRBE environment.



(a) DF receiver (IF = intermediate frequency)

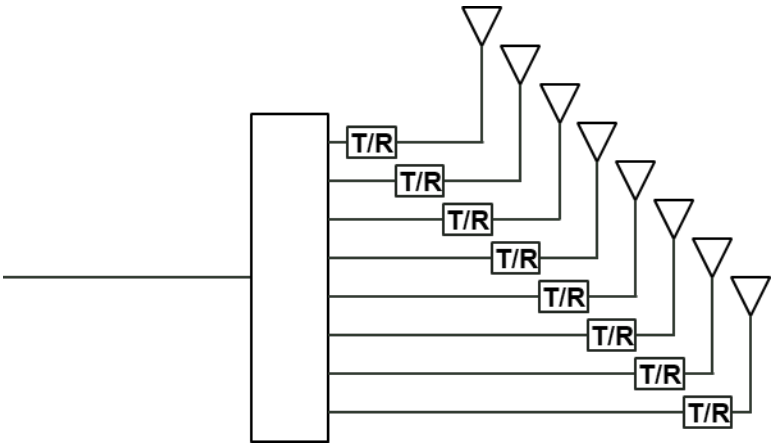


(b) Monopulse receiver



(c) Passive array radar

Fig. 3 Notional multiport SUT block diagrams



(d) Active array radar

Fig. 3 Notional multiport SUT block diagrams (continued)

DRBE's primary goal of creating a virtual test range for radar and EW systems leads to consideration of frequency coverage for the RF interface. Table 2 shows the standard Institute of Electrical and Electronics Engineers (IEEE) radar frequency bands and specific frequency assignments for International Telecommunications Union (ITU) Region 2 (North and South America).[2] The RF interface design should ensure primary coverage of these ITU radar bands up to X-band while meeting DRBE SUT performance requirements. A secondary goal will address continuous coverage consideration from near-DC to at least X-band, and possibly up to Ku-band.

Table 2 IEEE standard radar bands

Band designation	Nominal frequency range	Specific frequency range for radar based on ITU assignments for Region 2
VHF	30–300 MHz	138–144 MHz, 216–225 MHz
UHF	300–1000 MHz	420–450 MHz, 890–942 MHz
L	1–2 GHz	1215–1400 MHz
S	2–4 GHz	2300–2500 MHz, 2700–3700 MHz
C	4–8 GHz	4200–4400 MHz, 5250–5925 MHz
X	8–12 GHz	8.5–10.68 GHz
Ku	12–18 GHz	13.4–14.0 GHz, 15.7–17.7 GHz

4. RF Interface Conceptual Design

The primary function of the RF interface, shown in Fig. 4, is to provide interconnections between the analog SUTs and the digital RT-HPC. The RF interface will provide signal conditioning, up/down-conversion, and digital control interface between the SUTs and RT-HPC. The signal conditioning will include some combination of variable gain/attenuation and filtering. The DACs/ADCs

following the RF interface will convert the analog SUT signals to/from the digital domain. Multiple DRBE RT-HPC ports may be used for SUTs with larger IBW than the RF interface can handle; multiport SUTs are discussed in more detail in subsequent sections. The digital control interface will exchange information with the RT-HPC via an API. The RF interface will be configured for each of the connected SUTs prior to the start of the scenario. The interface may receive updates during the scenario progression to maintain performance required by the SUT.

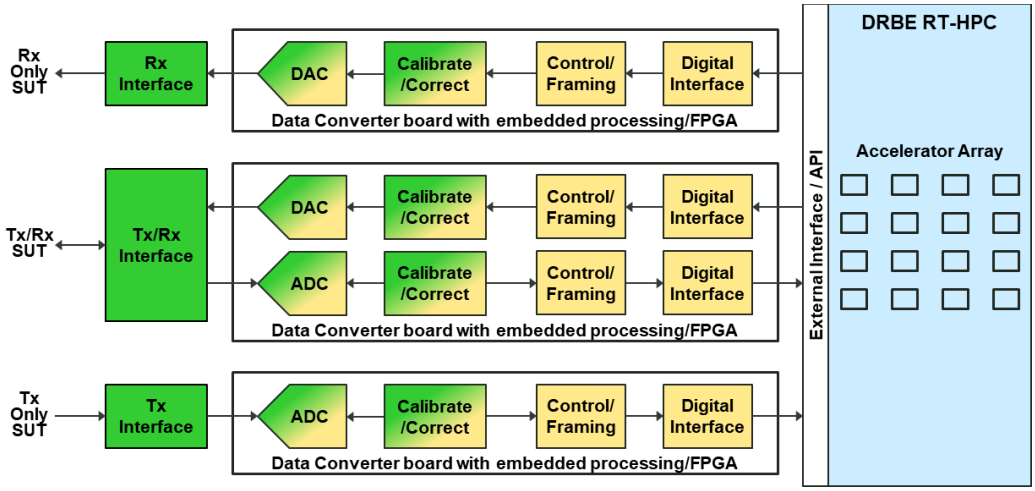
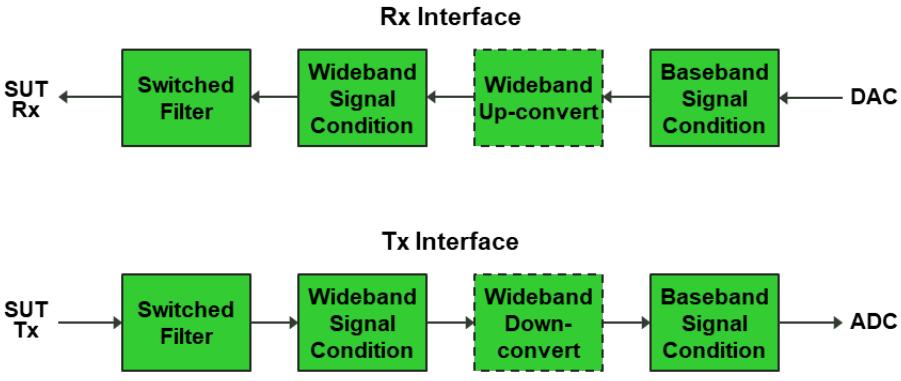
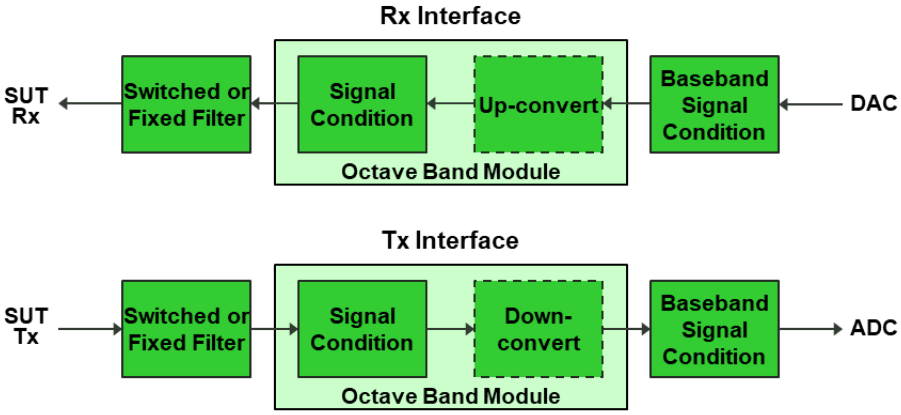


Fig. 4 Interfacing to the RT-HPC

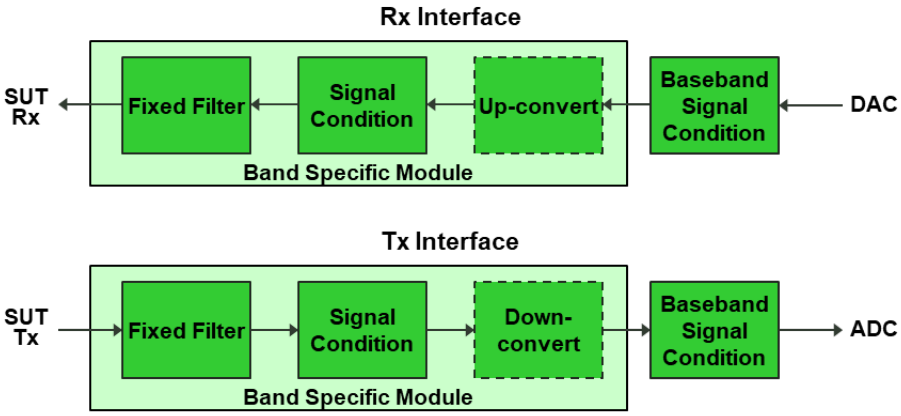
A modular RF architecture is preferred for interfacing with a wide variety of SUTs to the DRBE RT-HPC. The SUTs are expected to operate over a wide range of signal characteristics, such as overall frequency coverage, instantaneous bandwidth, signal amplitude, and dynamic range. Narrowband filtering in the RF interface is undesirable due to its potential impact on latency through the RF interface. Figure 5 shows three potential options (5a–c) for implementing the RF interface.



(a) Wideband



(b) Octave band



(c) Band-specific

Fig. 5 Modular RF interface options

The first option is a wideband architecture, shown in Fig. 5a, that would provide a single RF interface capable of accommodating all of the SUTs envisioned for the DRBE environment. A switched filter bank selects the frequency band of operation followed by wideband signal conditioning and up/down-conversion if necessary. There are drawbacks to this option. One is that it would require a large switched filter bank. In addition, wideband components typically have lower performance than narrower-band components.

The second option is an octave-band architecture, shown in Fig. 5b. It would replace the wideband signal conditioning and up/down-conversion components in Option 4a with octave-band components that are more readily available and typically offer improved performance over wideband components.

The third option is band-specific architecture, shown in Fig. 5c, that would require a large number of unique designs to accommodate all the SUTs. A fixed filter would select the frequency band of operation followed by optimal bandwidth signal conditioning and up-/down-conversion if necessary. Multiple unique designs would be required for this option, but it should offer better performance because the components can be selected to optimize performance for the specific frequency band of operation.

The RF interface should operate the data converters within their optimal voltage range to maximize dynamic range. Signal conditioning for all of the options should include variable gain/attenuation to convert the between the signal level of the SUT and an appropriate level for the data converters. The variable gain/attenuation range may need to be different in the Tx and Rx interfaces to match the SUT/data-converter signal levels. An LNA may be needed in the Rx RF interface to meet sensitivity requirements of the SUT. A high-power attenuator or directional coupler may be needed in the Tx RF interface to handle high-power incidents from a specific SUT and reduce the signal level into the RF interface. The instantaneous dynamic range of the RF interface should meet or exceed the dynamic range of the data converters. Careful RF interface design will seek to mitigate any degradation to the dynamic range due to the signal conditioning and up-/down-conversion stages. Up-/down-converters should provide a nominal intermediate frequency (IF) that falls within the frequency range of the data converter.

Options 4b and 4c can be designed as printed circuit boards for the different frequency bands that can be plugged in as a daughter card to the ADC/DAC board. This will allow simple reconfiguration of the RF interface to accommodate scenarios with different configurations of SUTs.

The RF interface's modular architecture should be capable of interfacing to SUTs with multiple RF inputs/outputs and include port-reduction techniques to minimize

the number of DRBE RF ports required. Port-reduction hardware will supplement the RF interface to interface to SUTs shown in Fig. 3 while fully capturing the functionality of the SUT. Port-reduction hardware, shown in Fig. 6, may require some combination of adjustable amplitude, phase, and possibly time delay to meet requirements of the SUTs.

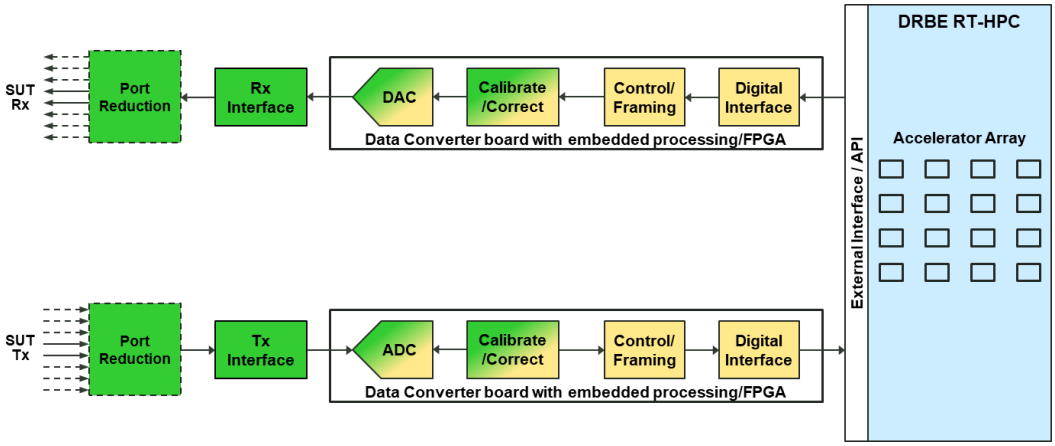


Fig. 6 Port reduction

A notional port-reduction example is shown in Fig. 7 for a four-element DF receiver. Variable phase shifters are shown in the example but could be replaced by adjustable time delay if desired. Photonic solutions implementing adjustable time delay may be feasible but require additional research. Optional variable gain is shown to compensate for gain differences in the channels. Port reduction for Tx SUTs and scaling to larger numbers of ports will be explored in Phase 2 of the program.

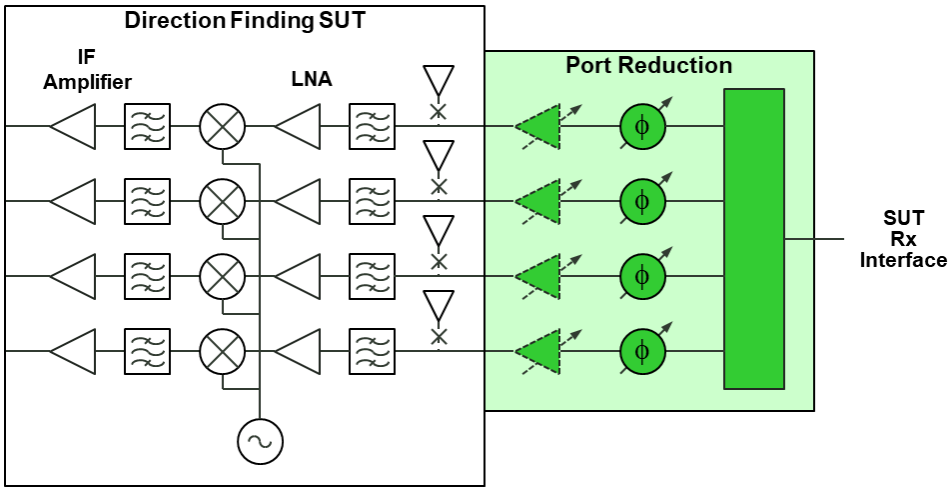


Fig. 7 Notional port reduction for DF SUT

5. High-Speed Data Converters

High-speed data converters are required to convert the SUT analog signal to a digital representation for input to the DRBE RT-HPC. Data-converter selection will primarily be driven by the DRBE average IBW requirement, nominally 1 GHz for Tx and 2 GHz for Rx, plus the SUT dynamic range. Other considerations for data-converter selection include form factor, availability, and cost. Hardware solutions including stand-alone ADC/DACs, Xilinx's RF system on chip (RFSoC), and DARPA's Hedgehog were considered in this study.

Sampling theory provides a basis for understanding how data converters operate and their capabilities and limitations. Data converters acquire/generate digital samples of an analog signal based on a sampling clock. The sampling clock frequency determines the highest frequency of the analog signal that can be sampled by the converter. Nyquist sampling theory specifies that the sampling clock must be greater than twice the highest frequency the analog signal in/out of the data converter to accurately represent the signal. The Nyquist criteria for sampled signals is shown in Eq. 1, where f_s is the sampling frequency and f_a is the highest frequency of the analog signal.[3]

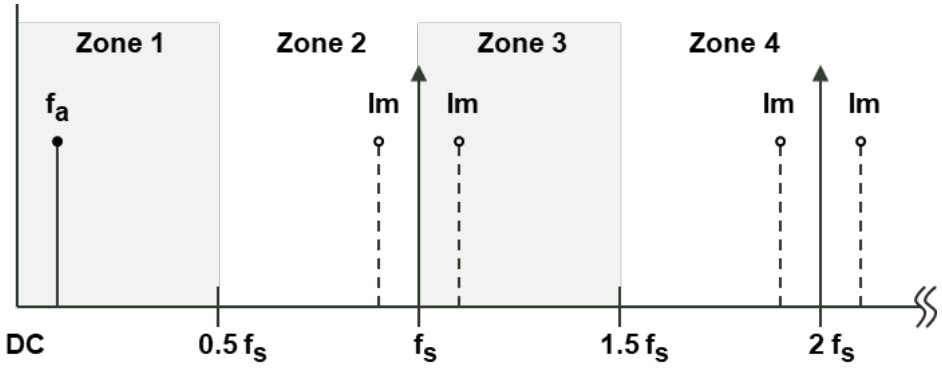
$$f_s \geq 2 \times f_a \tag{1}$$

The Nyquist bandwidth, also known as the first Nyquist zone, includes the frequency spectrum from *DC to* f_s */ 2*. Additional equally spaced Nyquist zones, with bandwidths equal to f_s */ 2*, extend beyond the first zone.

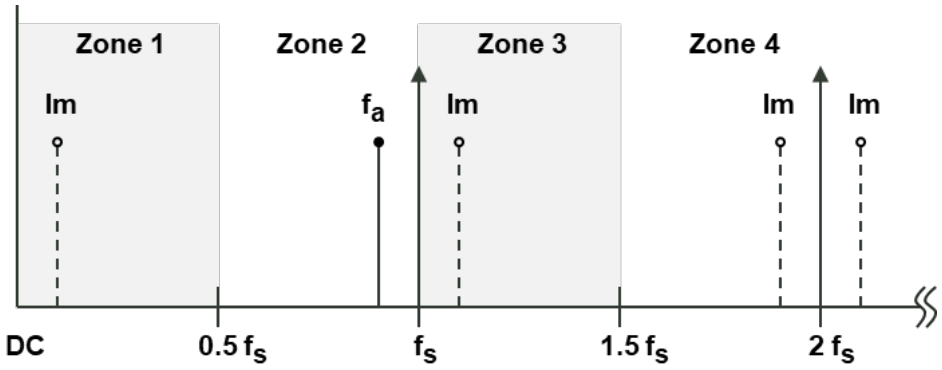
The sampled signals will produce aliased replicas, or images, that appear in other Nyquist zones of the frequency spectrum, at frequencies given by Eq. 2.[4] Harmonics and intermodulation distortion (IMD) products of the signal may also be present and can alias into other Nyquist bands as well.

$$\pm K f_s \pm f_a, where\ K = 1, 2, 3, \ldots \tag{2}$$

Figure 8 shows two examples of aliasing, including one where the Nyquist criteria were met and another where they were not. In Fig. 8a, with $f_a < f_s / 2$ in Nyquist Zone 1, the images appear in Nyquist Zones 2, 3, 4, …, while in Fig. 8b, with $f_a > f_s / 2$ in Nyquist Zone 2, the images appear in Nyquist Zones 1, 3, 4, …,.



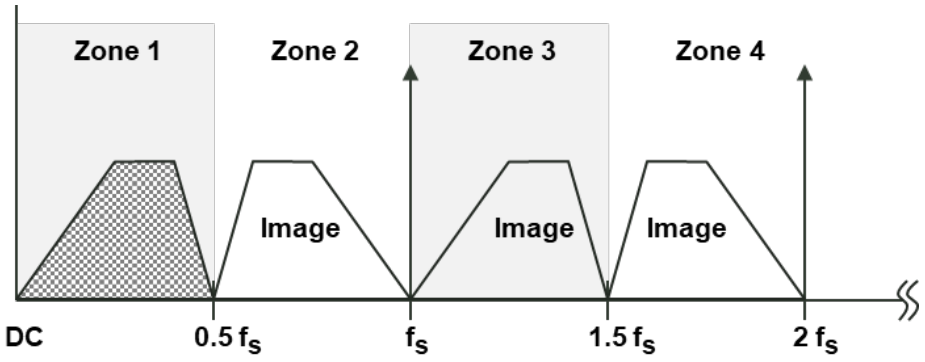
(a) Nyquist criteria met



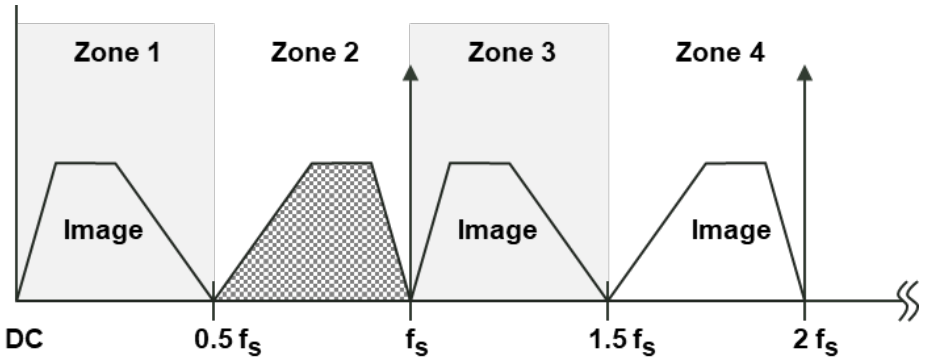
(b) Nyquist criteria not met

Fig. 8 Analog signal, f_a, sampled at f_s

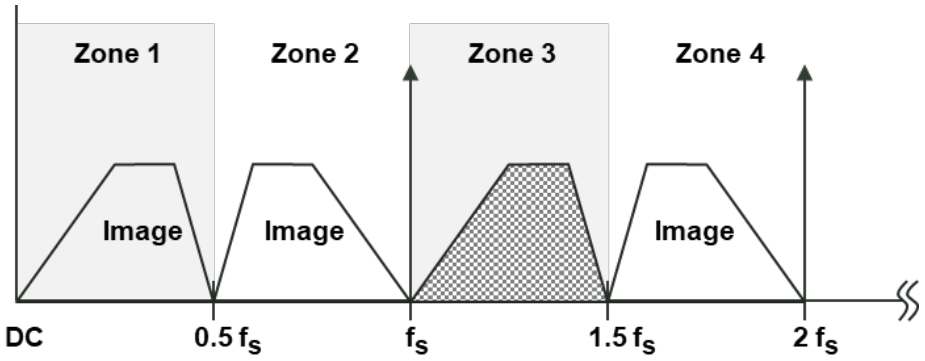
Aliasing in data converters can be advantageous using a technique referred to as undersampling, when the analog signal is sampled at less than the Nyquist criteria to effectively up-/down-convert the desired analog signal. Care must be taken when undersampling is used, as some of the image signals will appear reversed (mirror image) in the frequency spectrum. Figure 9a shows a sampled signal in the first Nyquist zone with the images falling in Zones 2, 3, and 4. Figure 9b shows a sampled signal in the second Nyquist zone with the images falling in Zones 1, 3, and 4. Figure 9 shows a sampled signal in the third Nyquist zone with the images falling in Zones 1, 2, and 4.



(a) Signal in first Nyquist zone



(b) Signal in second Nyquist zone



(c) Signal in third Nyquist zone

Fig. 9 Example undersampling

Anti-aliasing filters are typically used to minimize the impact of aliasing on system performance. Lowpass or bandpass filters can be used for signals falling in the first Nyquist zone, while bandpass filters are needed when undersampling signals in other Nyquist zones.

Time interleaving is a technique used to increase the effective sample rate in data converters. Multiple identical, lower-speed data converters are clocked at the same frequency as phase offsets based on the number of converters interleaved. The data

from each converter is multiplexed, or time-interleaved, to provide higher-frequency operation while maintaining the resolution of the individual converters. Interleaving produces additional artifacts in the frequency spectrum due to gain, phase, and offset mismatches between the converters.[5] The artifact frequencies are related to the number of data converters interleaved, the sampling frequency, and the signal frequency. Calibration may be used to mitigate the effect of the mismatches on performance.[6]

Nyquist sampling would require a minimum sampling rate of 2 Gsps for Tx and 4 Gsps for Rx to meet the DRBE average IBW requirement. Undersampling, where the signal is sampled at less than the Nyquist rate, should be considered in lieu of up-/down-conversion as long as it can provide sufficient performance for the SUT.

In sampling analog signals, the amplitude of the signal is quantized into discrete values, typically with a uniform step size and a finite set of levels based on the resolution, or number of bits, of the data converter, as shown in Fig. 10. These properties taken together specify the maximum dynamic range, and a quantization error is induced proportional to the step size.

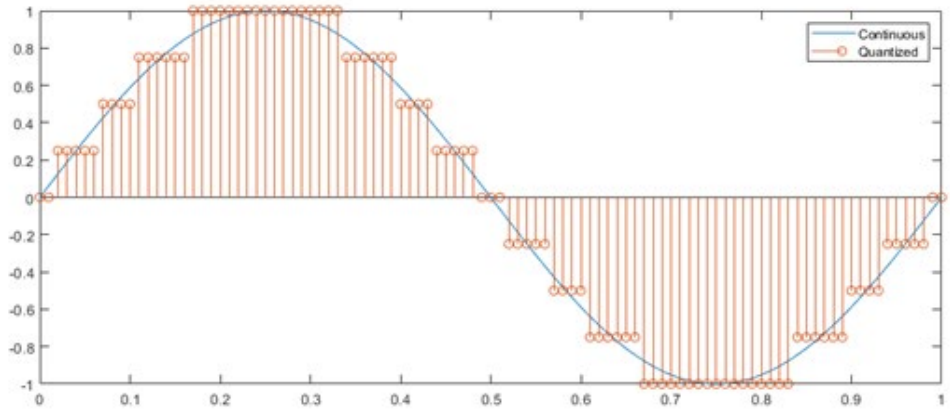


Fig. 10 Data converter quantization

To first order, this quantization error may be treated as additive white Gaussian noise (AWGN) uncorrelated to the signal that produced it.[7] Given that the quantization error is uniformly distributed across the least significant bit (typical) then, for a full-scale signal, we have that the ratio of signal to quantization-induced noise is given by

$$SQNR = 20\log_{10}(2^n) \approx 6n\ d \tag{3}$$

where n is the number of bits.

The quantization process also generates harmonics that fold into the instantaneous bandwidth of DRBE. These artifacts will propagate to any receive-capable SUT. The power level of the harmonics is primarily dependent on the number of quantization bits of the ADC (Table 3).[8]

Table 3 Quantization harmonic levels

	Harmonic power level relative to fundamental (dBc)					
Harmonic number	**1-bit**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
1	0.00	0.00	0.00	0.00	0.00	0.00
3	–9.54	–54.39	–67.01	–79.36	–91.57	–103.69
5	–13.98	–62.68	–73.30	–84.71	–96.46	–108.35
7	–16.90	–60.35	–73.57	–86.30	–98.71	–110.94
9	–19.08	–70.47	–79.50	–90.31	–101.80	–113.57
11	–20.83	–63.13	–76.78	–89.92	–102.42	–114.75

Note: dBc = decibels relative to the carrier

The harmonic power levels fall below that of the predicted signal-to-quantization-noise ratio (SQNR); however, harmonics would integrate over time unlike the AWGN-like behavior of the quantization noise. These artifacts may affect SUTs with long integration times (>1 s).

The initial quantization step in DRBE maps a continuous value to a fixed-point value; however, the back-end DRBE system processes signals as 32-bit floating-point numbers. This entails both a *fixed -> float* and *float -> fixed* conversion. The first conversion incurs additional albeit negligible quantization error as the 32-bit floating-point number has a mantissa of 23 bits, which by itself yields a higher-precision step size than the 8- to 16-bit output of a prospective ADC. The *float -> fixed* conversion will, however, yield similar SQNR and harmonic artifacts to those described for the ADC.

The outdoor environment for typical radar and EW systems has a very large dynamic range, its upper-end limited by the breakdown voltage of electricity in air. DRBE is tasked to emulate this environment but only from the perspective of the connected SUTs, which makes this a more tractable task. For the simplest DRBE scenario, a single path between a Tx SUT and an Rx SUT, this is achieved in a relatively straightforward manner: The Tx SUT transmits over some specified dynamic range (DR), shown in Fig. 11 as $(SUT)_{tx}$. At a bare minimum, DRBE must meet or exceed the DR of the transmit SUT as well as align its DR on that of the Tx SUT using amplifiers/attenuators/conditioning. It is expected that the DR of DRBE's transmitter will meet or exceed that of the DRBE receiver. Therefore, DRBE may accurately play back the signal to the receive SUT.

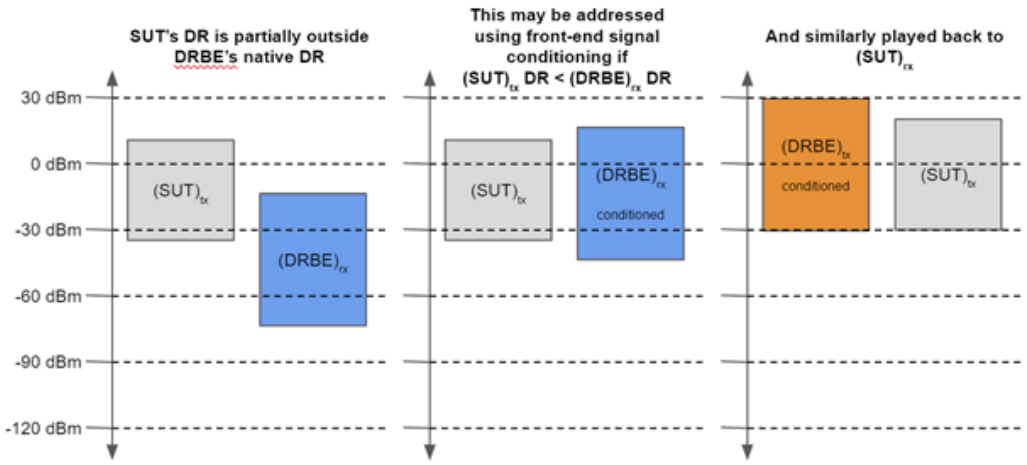


Fig. 11 SUT dynamic range alignment

However, this is complicated when there are two Tx SUTs. Each SUT may be sampled with fidelity using dedicated DRBE channels as before. However, playing those signals back to a single Rx SUT using a single DRBE channel will prove challenging when the span of the dynamic range of those two signals exceeds the DR of DRBE on Tx. In those situations, it may be required to dedicate multiple DRBE channels along with additional external hardware to support a larger DR.

Spurious free dynamic range (SFDR) is another measure of dynamic range that relates the amplitude of the highest spurious signal to the desired signal.[9] The amplitudes are generally given in root mean square (RMS) values. SFDR can be specified as decibels relative to full scale of the converter or decibels relative to the carrier.

To meet DRBE SUT dynamic range requirements, the resolution for both Tx and Rx data converters should be maximized while minimizing distortion products generated in the RF interface and data converters.

A survey of COTS data converters capable of meeting a 2-Gsps or higher sampling rate and 12 or more bits of resolution was completed. The survey included individual ADCs, DACs, and combination ADC/DACs in various formats including chip, board, and rack-mount chassis. Board-level formats, including PCIe, PXIe, AXIe, and mezzanine card, are available from various suppliers. Figure 12 shows plots of sample rate versus resolution for COTS chip and board/chassis-level ADCs/DACs found in the survey.

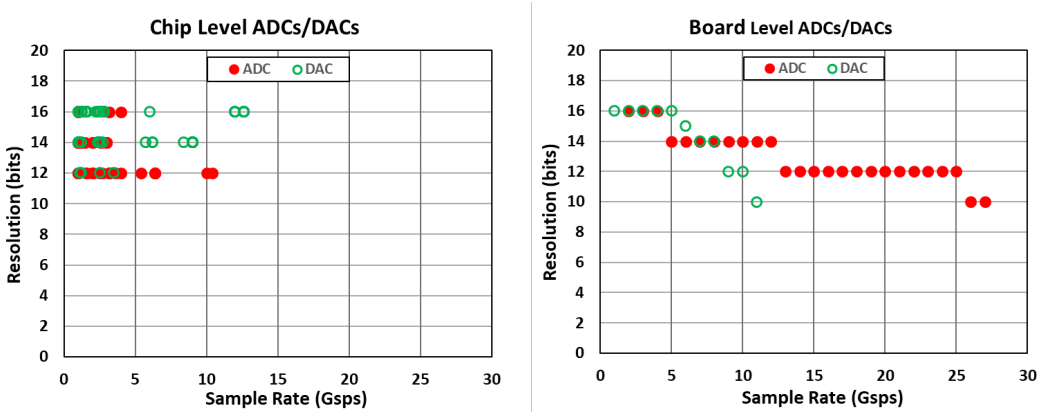


Fig. 12 COTS ADCs/DACs

Xilinx RFSoC is a relatively new product line that integrates several multi-Gsps data converters with processors, Ultrascale+ programmable logic, double-data-rate memory, and various peripherals in a system-on-a-chip architecture. The RFSoC includes a quad-core ARM Cortex A53 application processor and a dual-core ARM Cortex R5 processor for real-time processing. RFSoC peripherals include PCIe Gen2, USB 3.0, SATA 3.0, DisplayPort, GigE, and SD/SDIO. There are currently three generations of RFSoC products, each available in different speed grades, with select devices and specifications shown in Table 4.[10]

Table 4 Xilinx RFSoC specifications

Specification	ZU28DR	ZU29DR	ZU39DR	ZU48DR	ZU49DR
Generation	1	1	2	3	3
No. of ADCs/DACs	8/8	16/16	16/16	8/8	16/16
ADC/resolution (bits)	12	12	12	14	14
ADC sample rate (Gsps)	4.096	2.058	2.222	5	2.5
DAC resolution (bits)	14	14	14	14	14
DAC sample rate (Gsps)	6.554	6.554	6.554	10	10
RF input frequency (GHz)	4	4	5	6	6

As shown in Table 4, the RFSoC input frequency range extends beyond the Nyquist sampling criteria allowing operation in the second Nyquist zone. Special features are built into the DAC architecture to flatten the normal Sin(x)/(x) response in the first Nyquist zone as well as boost the response in the second Nyquist zone.[11] The RFSoC DAC is capable of higher Nyquist zone operation but will suffer from Sin(x)/(x) roll-off in frequency response. RFSoC evaluation boards are available from Xilinx, and many board-level products are available from several vendors in different form factors, including mezzanine card, module, cPCI, PCIe, and VPX.

DARPA Hedgehog[12] is a wideband, multichannel, software-defined radio (SDR) that can be rapidly reconfigured for a variety of applications. The Hedgehog SDR

integrates a Microwave Array Technology for Reconfigurable Integrated Circuits transceivers chip with a first-generation Xilinx RFSoC (ZU29DR). Hedgehog can be configured with 4–8 Tx/Rx channels that operate over 20 MHz to 40 GHz with 2 GHz IBW per channel. While the reconfigurable transceiver capability of the Hedgehog is attractive for DRBE, the first-generation RFSoC ADC sampling rate of 2.058 Gsps may ultimately limit its performance.

6. RF Interface Frequency Planning

Frequency planning is an important phase in the RF design process to ensure performance requirements can be met. Nonlinear RF components can generate a variety of harmonics and IMD products that may degrade performance. Careful frequency planning can mitigate these effects by moving the nonlinear products away from the frequency band of interest where they can more easily be filtered if needed. Many software tools are available to assist in the RF-frequency-planning process.

The data representation for the DRBE RT-HPC will be digital in-phase/quadrature-phase (I/Q) data. Analog I/Q demodulation is typically used to generate the I/Q signals that can then be digitized but requires precise amplitude and phase control to achieve good image rejection (>50 dB). The best-performing analog I/Q demodulators can achieve around 60–70 dB for certain frequency bands. Current-generation ADCs/DACs sample fast enough to support digital I/Q demodulation over the DRBE IBW and, in contrast to analog I/Q demodulation, provide image rejection exceeding 100 dB across the bandwidth.

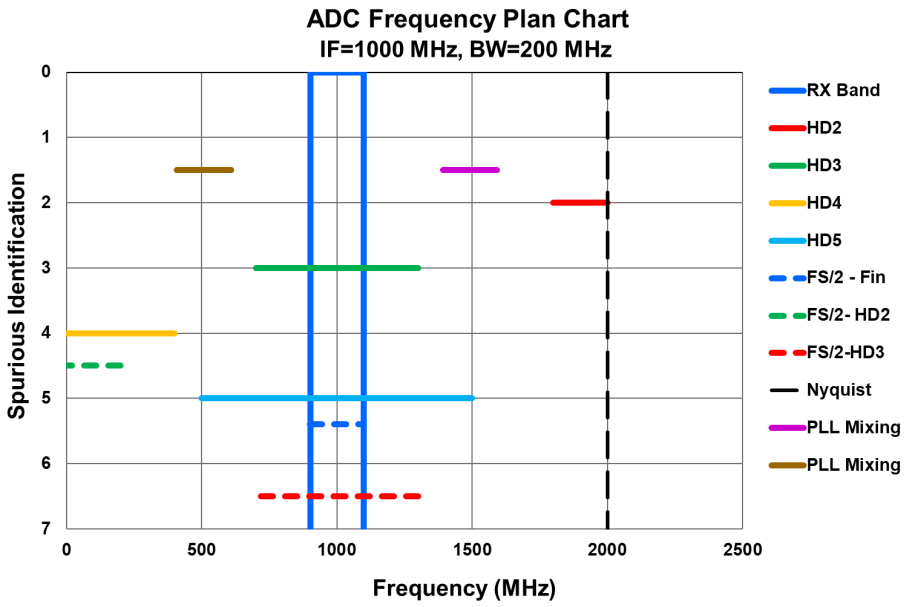
The data converter specifications are important in the frequency planning process because they set the limits on the IF that can be processed. The data converter requirements are determined by a combination of the IF and the SUT input/output frequency to the RF interface. A notional frequency plan spreadsheet for the ITU radar frequency bands is shown in Fig. 13 with a sample rate of 4 Gsps. The spreadsheet calculates the first and second Nyquist zones and the local oscillator frequencies needed for up-/down-conversion. This example sets a fixed IF of 1000 MHz and limits the usable frequency range to 90% of the Nyquist bandwidth (BW), 2 GHz, to allow for filtering. The cells are color-coded to indicate if the frequencies are within the calculated Nyquist and up-/down-conversion bands. As shown in Fig. 13, the radar bands up to L-band fit within the first Nyquist zone and the S-bands fit within the second Nyquist zone. There are some tradeoffs associated with using the second Nyquist zone that must be considered in the final design. Since X-band exceeds the Nyquist BW, it must be split into two bands, X low and

X high, as shown in the example. Another option to accommodate X-band is to use higher-sampling-rate data converters.

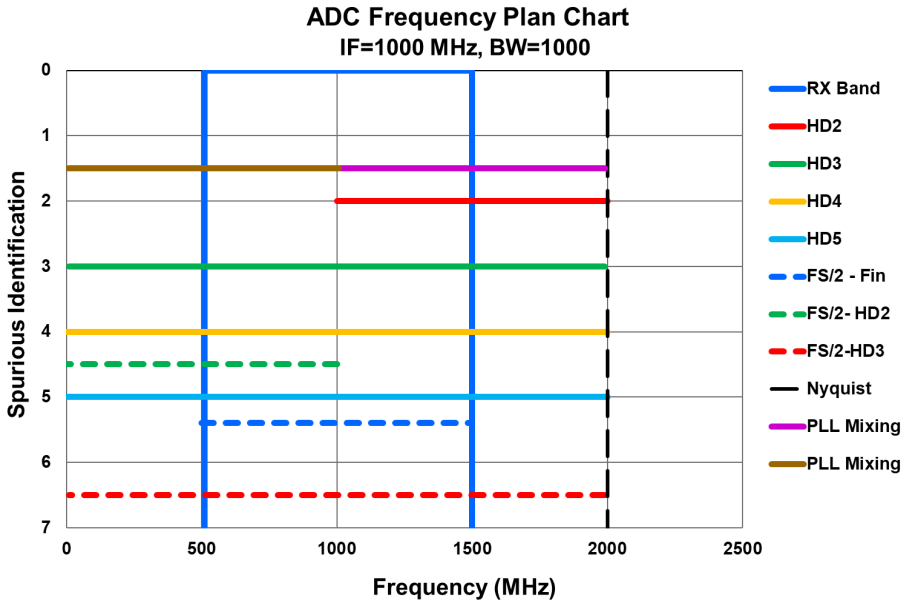
	1st Nyquist				2nd Nyquist			Up-convert				High Side Down-convert			
Band	Fmin	Fc	Fmax	BW	Fmin	Fc	Fmax	IFmin	IFc	IFmax	LO	IFmin	IFc	IFmax	LO
	100	1000	1900	1800	2100	3000	3900	100	1000	1900		100	1000	1900	
VHF	138	141	144	6											
VHF	216	235.5	255	39											
UHF	420	435	450	30											
UHF	890	916	942	52											
L	1215	1308	1400	185											
S	2300	2400	2500	200	2300	2400	2500	900	1000	1100	1400	900	1000	1100	3400
S	2700	3200	3700	1000	2700	3200	3700	500	1000	1500	2200	500	1000	1500	4200
C	4200	4300	4400	200	4200	4300	4400	900	1000	1100	3300	900	1000	1100	5300
C	5250	5588	5925	675	5250	5588	5925	662.5	1000	1338	4588	662.5	1000	1338	6588
X Full	8500	9590	10680	2180	8500	9590	10680	-90	1000	2090	8590	-90	1000	2090	10590
X Low	8500	9045	9590	1090	8500	9045	9590	455	1000	1545	8045	455	1000	1545	10045
X High	9590	10135	10680	1090	9590	10135	10680	455	1000	1545	9135	455	1000	1545	11135

Fig. 13 Frequency planning spreadsheet

Frequency planning for the data converter should maximize the BW available while minimizing the harmonic and image frequencies that fall within the frequency band of interest. Figure 14a shows notional results for an ADC using the Xilinx frequency planner tool[13] with an IF centered at 1000 MHz and a moderate BW of 200 MHz, with some of the harmonic products and images falling into the Rx band of interest. Figure 14b highlights the difficulty in achieving wideband performance with a BW of 1000 MHz, as all of the harmonic products and images to fifth-order fold back into the Rx frequency band of interest. These plots do not show the full picture because they do not include the amplitude level of the harmonic/image products. In general, lower-order harmonics have higher power levels relative to the signal of interest. The spurious performance specifications, typically expressed in decibels relative to carrier, can typically be found in the converter data sheet. The narrowband ADC performance can be further improved by shifting the IF to move the harmonic products out of the Rx frequency band of interest, as shown in Fig. 14c.

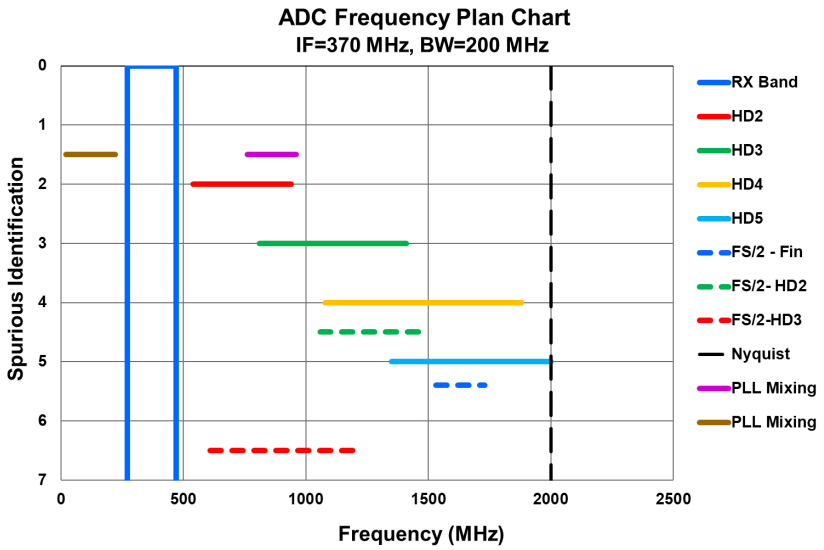


(a) Narrowband



(b) Wideband

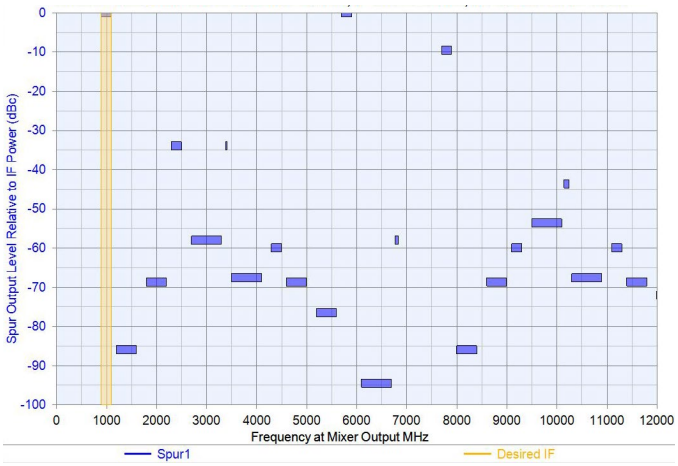
Fig. 14 Notional data converter frequency plan



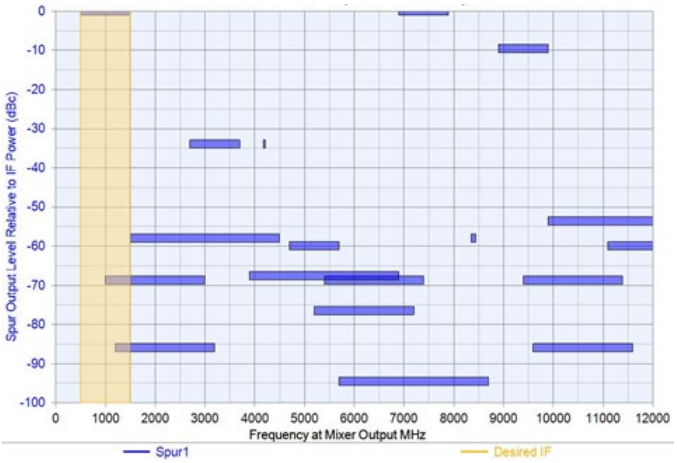
(c) Narrowband with IF at 370 MHz

Fig. 14 Notional data converter frequency plan (continued)

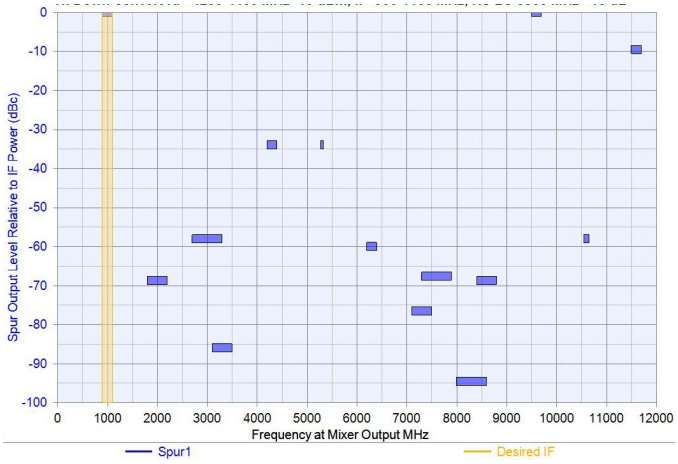
The frequency plan for the up-/down-conversion stage(s) should seek to minimize the harmonic and spurious products that fall within the frequency band of interest and maximize dynamic range in/out of the data converters. Keysight's SystemVue includes a frequency planner tool called WhatIF[14] to assess various schemes. Figures 15a–f shows notional down-conversion frequency plans for the S, C, and X radar bands with an IF of 1000 MHz and RF input level of –10 dBm. The simulations were done using the built-in Watkins–Johnson mixer model to calculate the IMD products. These preliminary simulations show reasonable performance with the worst-case IMD products around –57 dBc in the frequency band of interest. Fine-tuning can be completed in the design phase by adjusting the IF and RF input power level to optimize performance.



(a) S-band 2300–2500 MHz

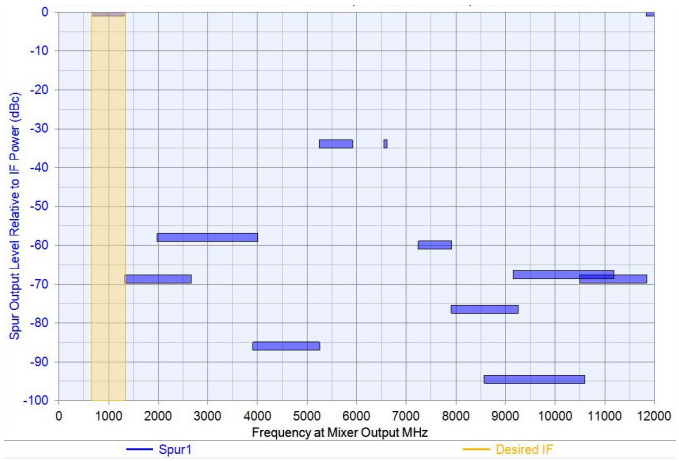


(b) S-band 2700–3700 MHz

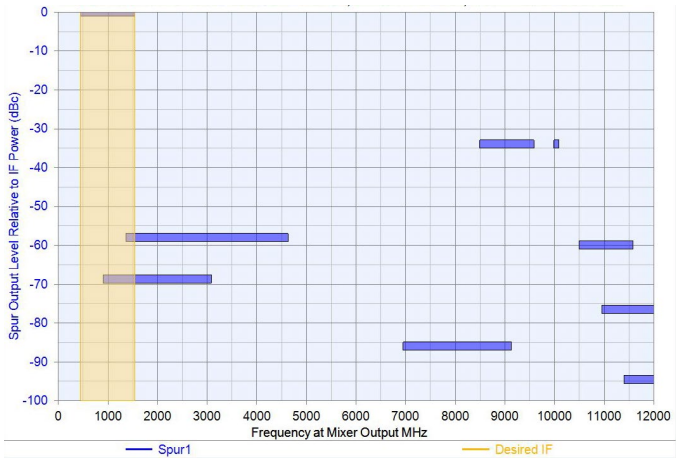


(c) C-band 4200–4400 MHz

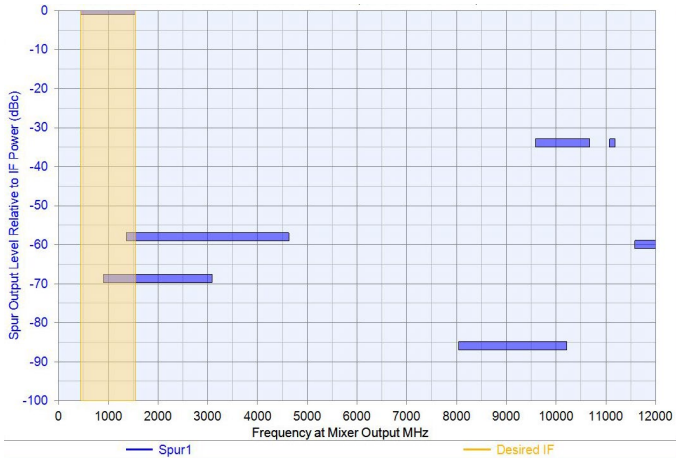
Fig. 15 Notional down-conversion frequency plan



(d) C-band 5250–5925 MHz



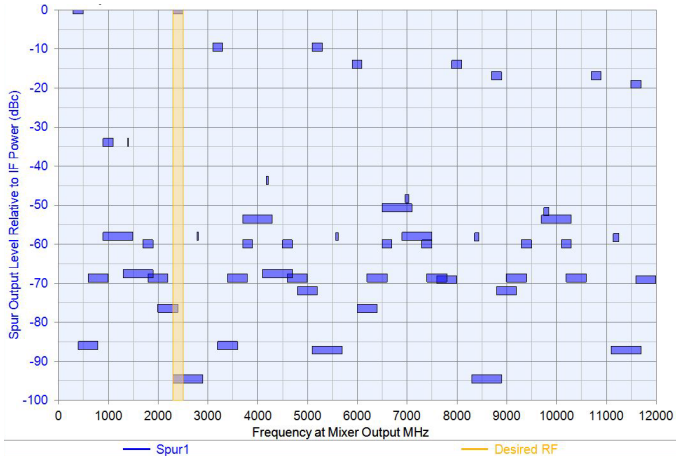
(e) X-band low 8500–9590 MHz



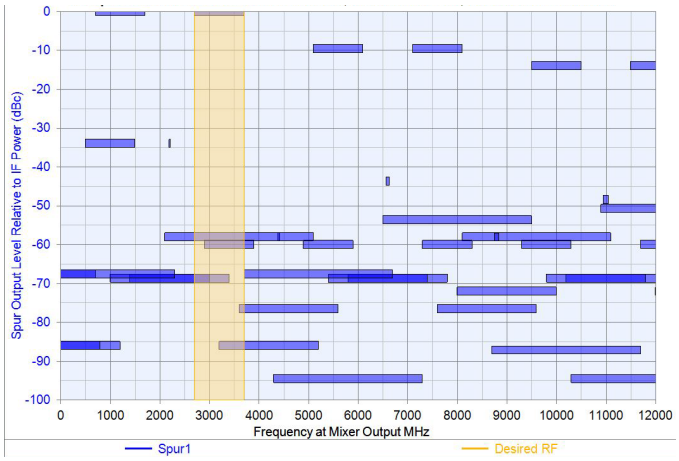
(f) X-band high 9590–10680 MHz

Fig. 15 Notional down-conversion frequency plan (continued)

Figures 16a–f shows notional down-conversion frequency plans for the S, C, and X radar bands with the same IF of 1000 MHz and RF input level of –10 dBm. The simulations were also done using the built-in Watkins–Johnson mixer model to calculate the IMD products. These preliminary simulations show reasonable performance with the worst-case IMD products around –57 dBc in the frequency band of interest. Fine-tuning can be completed in the design phase by adjusting the IF and RF input power level to optimize performance.

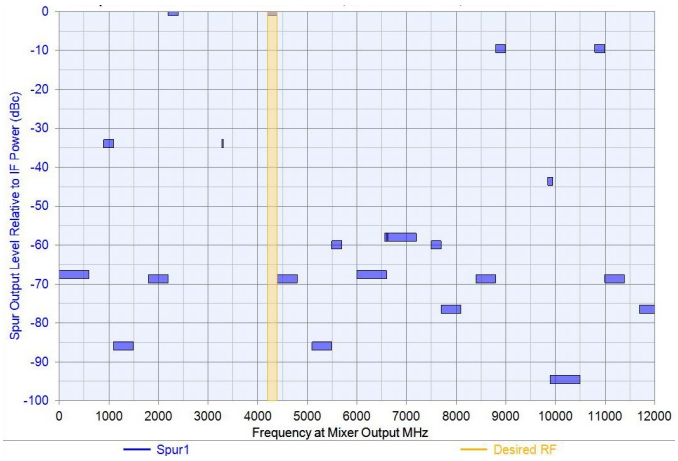


(a) S-band 2300–2500 MHz

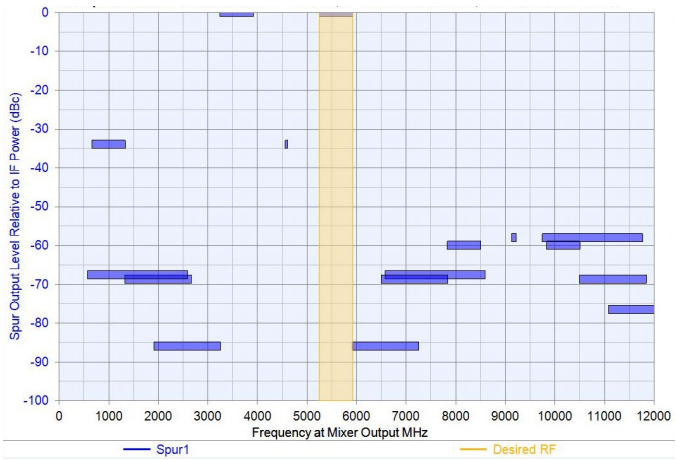


(b) S-band 2700–3700 MHz

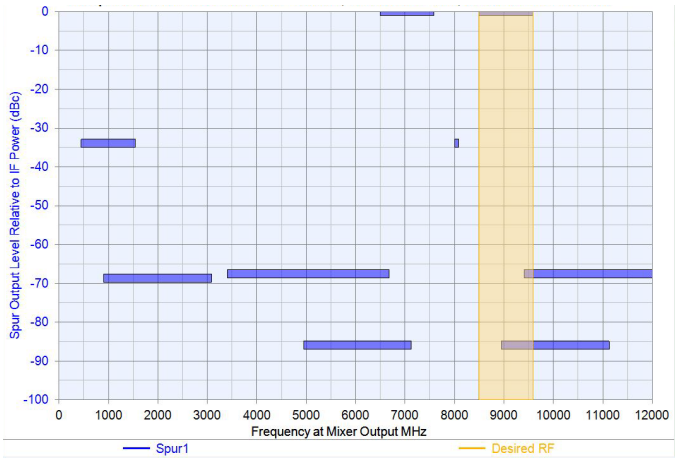
Fig. 16 Notional up-conversion frequency plan



(c) C-band 4200–4400 MHz

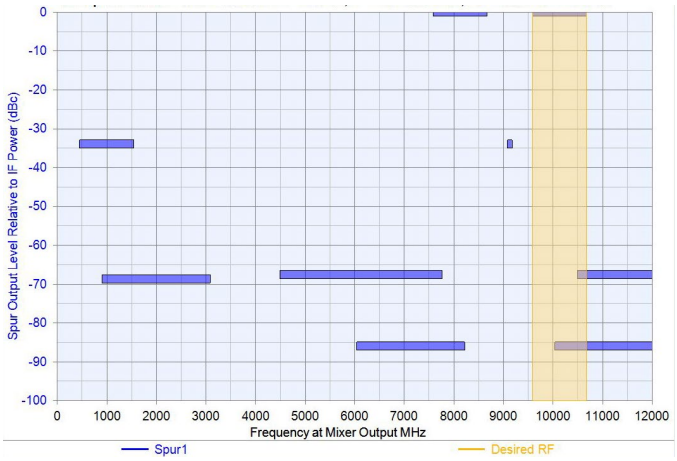


(d) C-band 5250–5925 MHz



(e) X-band low 8500–9590 MHz

Fig. 16 Notional up-conversion frequency plan (continued)



(f) X-band high 9590–10680 MHz

Fig. 16 Notional up-conversion frequency plan (continued)

7. Data Converter Clock Generation and Distribution

The high-speed data-converter sampling clock is a critical component in the DRBE system because it will affect the overall performance. The sampling clock sources considered for this function require multigigahertz operation to meet the DRBE bandwidth requirements and should have excellent stability including low-phase noise and jitter. Phase noise and jitter are essentially the same parameter, with phase noise being the frequency domain representation while jitter is in the time domain.

Phase noise of the clock source is important because it can negatively affect radar performance by masking lower-level return signals, rendering them undetectable. Phase noise is caused by random, short-term variations in the phase of a signal and appears as noise sidebands in the frequency domain. Phase noise is typically measured as the spectral density in a single sideband of the signal and expressed in decibels relative to carrier/hertz. Phase noise can be approximated by a piecewise linear function when plotted versus log (f), as shown in Fig. 17.

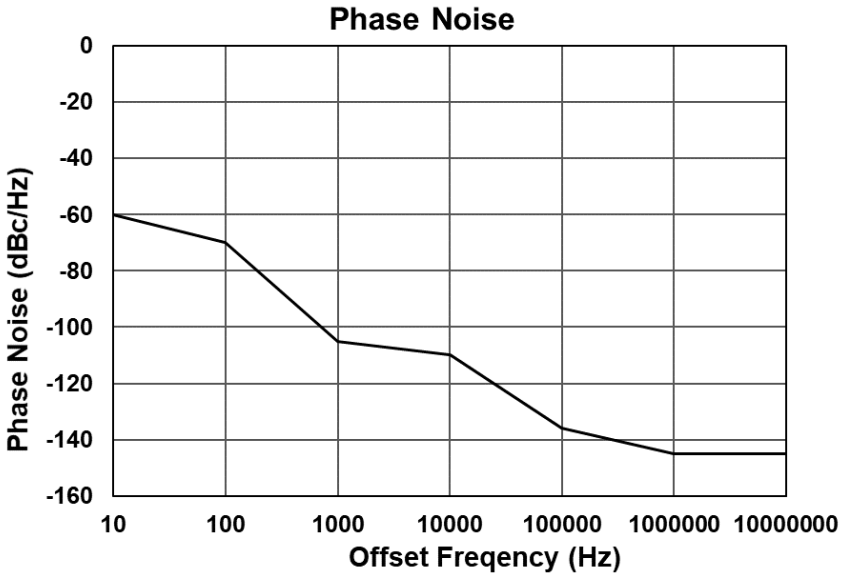


Fig. 17 Piecewise linear phase-noise approximation

Clock jitter will affect the ability to align the streaming data to the RT-HPC across the data converters for all of the SUT channels in the scenario. The random, short-term variations in phase associated with phase noise are also known as phase jitter. This deviation will change where the signal is sampled in time, resulting in an amplitude error. RMS phase jitter can be calculated from the phase noise given by Eq. 4, where A is the area under the piecewise linear phase-noise approximation shown in Fig. 17, and f_s is the sampling clock frequency. The RMS phase jitter can be converted to RMS time jitter in Eq. 5.[15]

$$RMS\ Phase\ Jitter\ (radians) = \sqrt[2]{2\ x\ 10^{A/10}} \tag{4}$$

$$RMS\ Jitter\ (seconds) = \frac{\sqrt[2]{2\ x\ 10^{A/10}}}{2\ \pi\ f_s} \tag{5}$$

Two options under consideration for the multigigahertz clock sources include lower-frequency oven-controlled crystal/surface acoustic wave (SAW) oscillators with integral multipliers and phase locked loop (PLL) synthesizers. Crystal/SAW oscillators are typically fixed-frequency and tend to have better stability, while PLLs offer the flexibility of tunable frequency at the expense of stability. Figures 18 and 19 show plots of phase noise and calculated jitter, respectively, for clock sources that could potentially meet the requirements for the data-converter sampling clock.

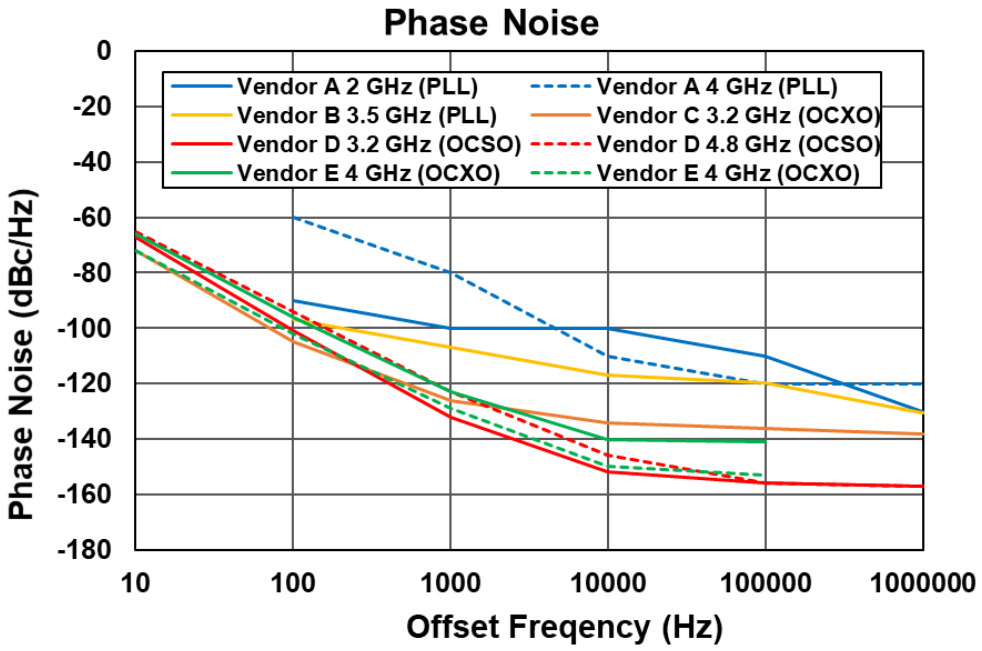


Fig. 18 Phase noise of selected clock sources

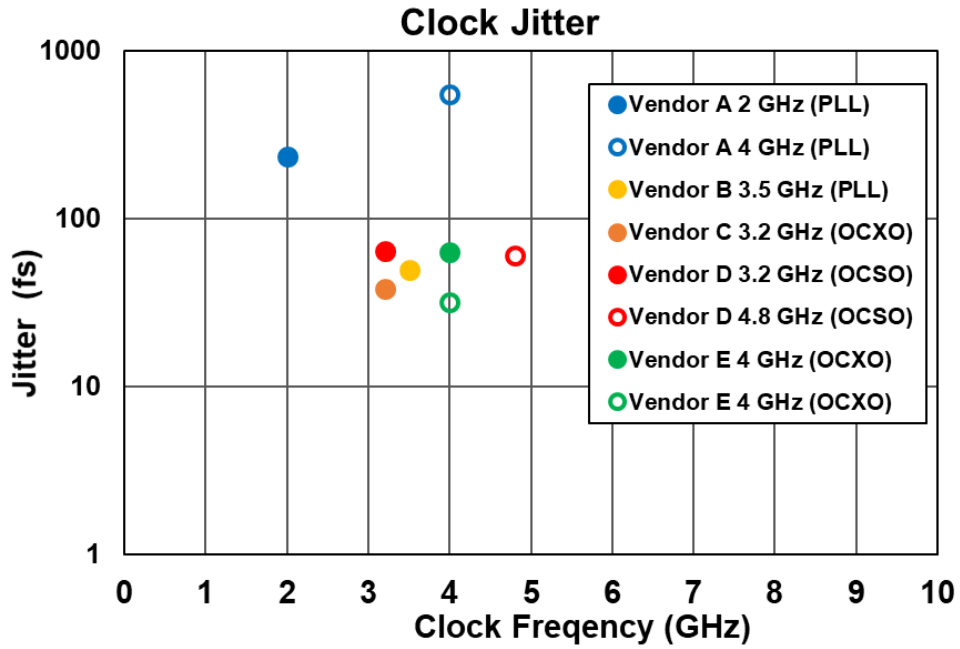


Fig. 19 Jitter of selected clock sources

RFSoCs have internal PLL clock generation capable of operating up to 10 GHz and multitile synchronization that may be useful if satisfactory timing performance can be achieved across the channels.

There are two potential methods for distribution of the data-converter clock. The high-frequency clock can be split N ways and distributed directly to the data converters, or a lower-frequency reference clock, such as 10 or 100 MHz, can be split and distributed to local high-frequency clocks close to the data converters. Many RF power splitters are available up to 16-way, covering 2–18 GHz with less than 0.1-dB amplitude and less than 1° phase imbalance. Phase-matched coaxial cables may be needed for connection between the splitter and data converter to minimize additional imbalance. Low-frequency reference-clock generation is generally easier to implement via direct splitting or clock-distribution-integrated circuits.

8. Built-In-Self-Test (BIST) and Calibration

Calibration and BIST ensures the overall health of the emulator and readiness to execute scenarios. The BIST verifies nominal system and subsystem operation and tests the RT-HPC, digital interfaces, ADCs/DACs, and the RF interface. Calibration aligns Rx and Tx channels across time, phase, and amplitude.

The DRBE system consists of many components, any of which might fail or incur damage. All critical paths, digital or RF, are included in the BIST. This means that all critical branching in the design (e.g., a switchable RF filter bank) must be individually tested. This approach ensures problems are not overlooked and issues may be isolated quickly, but it significantly increases the execution time of the BIST. To mitigate this, the BIST is executable in the following ways:

- *System-wide BIST*: All critical paths are tested for nominal operation, and a report is generated detailing pass/fail with measured results where relevant. This mode is executed on power-on and can be triggered at any point by the user.
- *Scenario BIST*: A representative and relevant sample of critical paths is tested for nominal operation. This mode is contextualized by a specific scenario, and the user can choose to execute this BIST at the beginning and/or the end of a scenario.
- *Individual BIST*: A user may trigger a BIST on a particular critical path and receive a detailed report.

What is measured and reported for each critical path of the BIST is specific to that path. The BIST does not characterize the critical path but verifies nominal operation. Some examples include the following:

- Subsystems receive and acknowledge commands.

- Power levels into and out of the ADCs/DACs are as expected across configurations of the RF front-end.
- Error rates between high-speed digital interfaces are within tolerance.

In contrast to the BIST, calibration characterizes and then aligns some subset of DRBE channels to a specified calibration plane across time, phase, and amplitude. Consider one of the foundational use cases, a single path (Fig. 20), where DRBE emulates a single path between two SUTs by applying a time offset, attenuation, phase offset, and a Doppler offset.

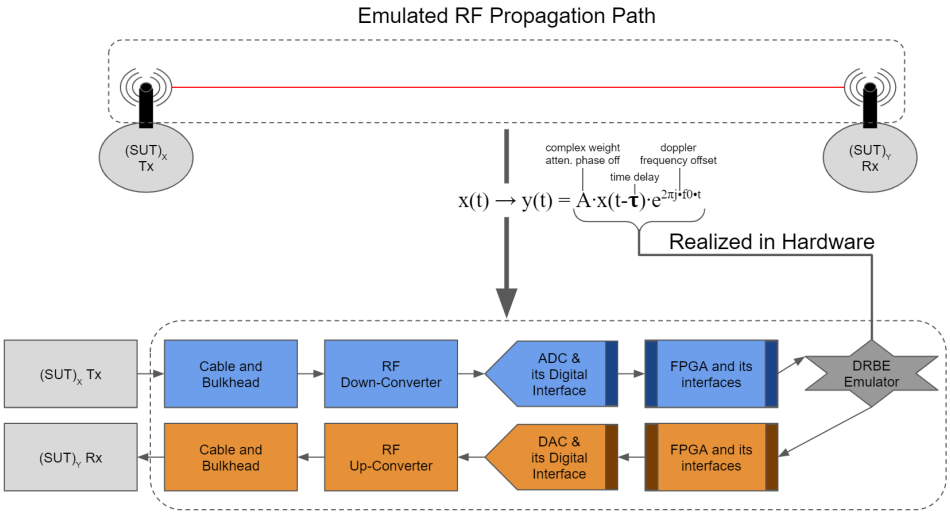


Fig. 20 Single path calibration

The addition of cables, an RF front-end, digital processing, and digital transfer all contribute to the time, phase, and amplitude of the signal. Some contributions are fixed, some may change from power cycle to power cycle, and yet others may update on retune depending on the particular hardware in question. In Fig. 21, it is assumed that temperature has reached steady state.

Fixed:	x	x	x	x
Power Cycle:		x	x	x
Retune:		x		

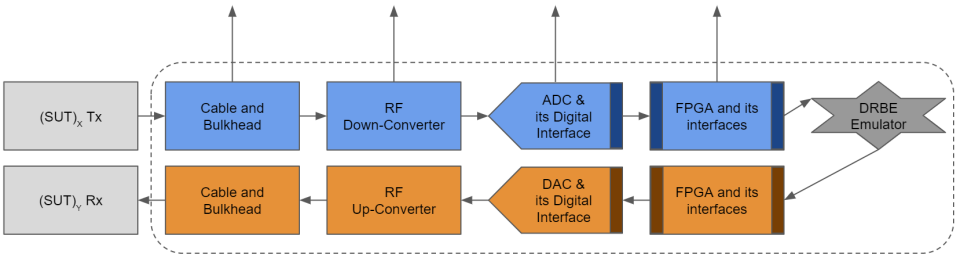


Fig. 21 Calibration considerations

This drives the requirement for a built-in calibration capability that executes during runtime. Ideally, all channels are aligned to the same calibration plane (Fig. 22).

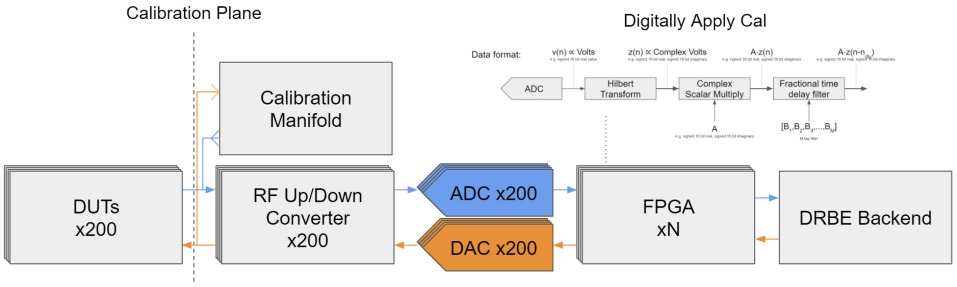


Fig. 22 Calibration plane

However, this imposes a significant challenge to implement, as all DRBE channels must route essentially to one location. The following considers aligning a subset N (where N~10) DRBE channels across time, amplitude, and phase.

A set of receivers may be aligned using a signal that falls coincident across the calibration plane. The signal is generated using a calibration manifold (a network of power dividers that has itself been calibrated). Once received, a reference channel is selected and all other channels cross-correlate their result to estimate the difference. This difference may then be used to apply a correction to align the receivers (Fig. 23).

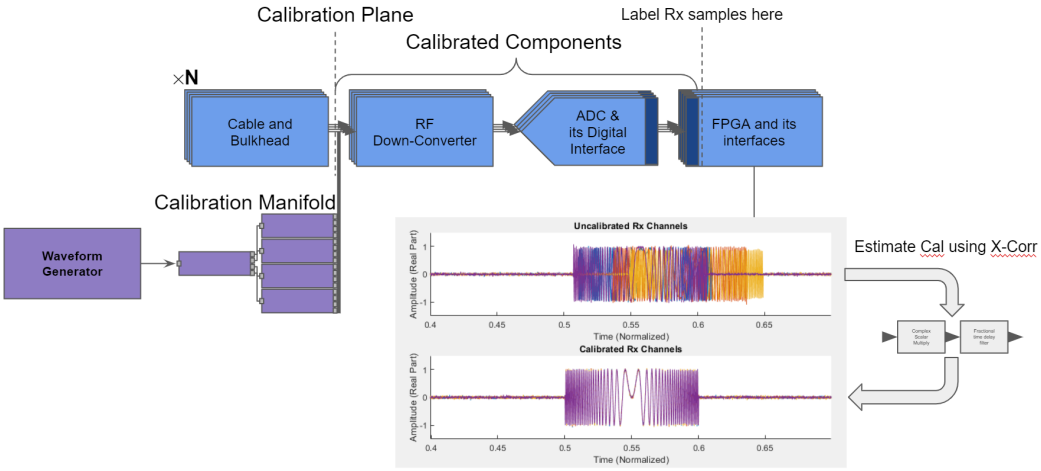


Fig. 23 Rx channel alignment

A set of transmitters may be simultaneously aligned by having each transmit a mutually orthogonal waveform (Fig. 24). The hardware setup is much the same as in the Rx case.

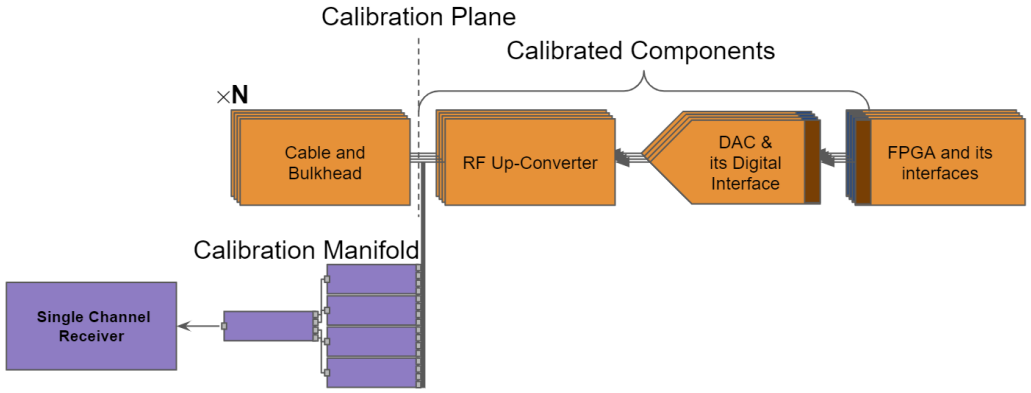


Fig. 24 Tx channel alignment

Moreover, the calibration processing may be done in parallel. This process is shown in Fig. 25 for 16 channels using sets of pseudo random noise (PRN) sequences, modulated using quadrature phase-shift keying, that have been additionally shaped to occupy a desired bandwidth and time slot.

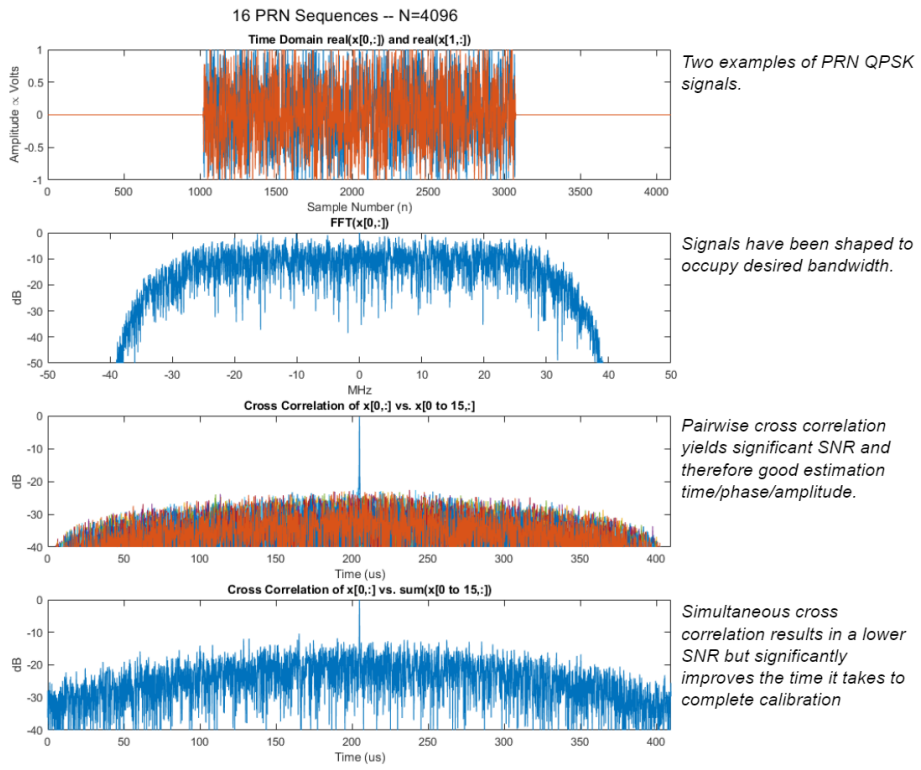


Fig. 25 PRN sequence Tx calibration

At a high level, longer PRN sequences improve signal-to-noise ratio (SNR), and adding additional channels reduces SNR. The quality of the calibration estimation is driven by the overall SNR of the cross-correlation result. Other types of orthogonality, such as using time slots, can mitigate SNR loss and allow for additional channels but comes at the cost of overhead and a priori knowledge of the coarse time offset between channels.

The last stage of calibration requires that the back-end of DRBE be characterized (Fig. 26).

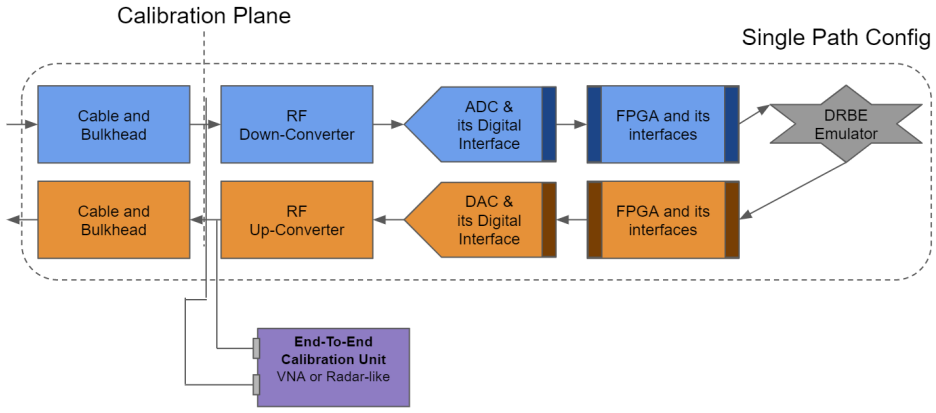


Fig. 26 End-to-end calibration

This accounts for contributions to time/phase/amplitude through the entire DRBE system and is critical to providing accurate target responses for radar-like SUTs. Figure 26 shows a traditional approach to end-to-end calibration and is hardware resource-intensive due to the requisite calibration unit. It is expected that there will be additional unused transceivers in the DRBE system that can be appropriated for this purpose, which reduces the impact to the system design. However, we propose investigating a modified end-to-end calibration approach (Fig. 27) where the calibration signal originates past the ADC (Field Programmable Gate Array [FPGA]).

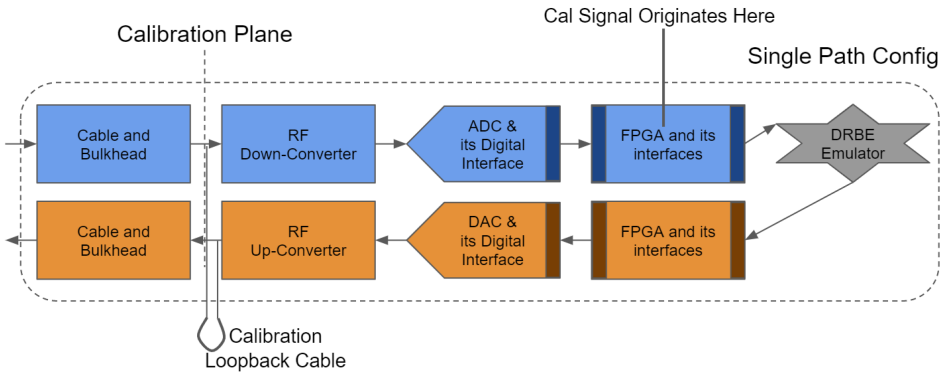


Fig. 27 Modified end-to-end calibration

No additional transceivers are needed for this approach—just a calibration path with known characteristics. Care must be taken to ensure that the calibration plane is not offset when applying this correction factor to DRBE.

The calibration plane has been placed after the cables and bulkheads in the previous figures; however, it is intended that those will be measured and accounted for as well. Since their contribution is fixed, it does not need to be included in the runtime calibration but will be applied to the final calibration.

9. Physical Interface to RT-HPC

The physical interface to the DRBE RT-HPC is described in the MIT-LL document DRBE Real-Time Streaming Data Interface.[16] Physical interface considerations include discussion on high-speed serial protocols; fiber-optic links; error detection, correction, and latency; and 100-gigabit Ethernet as reference implementation. Clock timing and timekeeping are also covered, including sampling and labeling data, wall time reference, and potential need for sampling-clock tracking atomic time. Interface specifications including clocking requirements, packet header and data format, and DAC arrival time tuning (elastic buffer) are also covered.

10. Application Programming Interface

The DRBE channel interface is described in the MIT-LL document DRBE Channel Interface Specification,[17] including details on messaging format, definitions, and concept of operations.

The DRBE RF interface will require information about the SUTs' operational parameters during initial scenario configuration (Table 5). Additionally, the RF interface will need to know if any of the relevant SUT operational parameters will be updated during the scenario.

Table 5 RF interface metadata parameters

Name	Units	Description
tx_freq	GHz	Transmit center frequency
tx_bw	GHz	Transmit total occupied BW
tx_pwr	dBm	Transmit power
#_tx_ports	…	Requires additional info on signal relationship between ports such as amplitude, phase, delay
tx_ant_gain	dBi	Transmit antenna gain
rx_freq	GHz	Receive center frequency
rx_bw	GHz	Receive total occupied BW
rx_pwr	dBm	Receive power
#_rx_ports	…	Requires additional info on signal relationship between ports such as amplitude, phase, delay
rx_ant_gain	dBi	Receive antenna gain

11. Surrogate SUT

Surrogate SUT hardware will be used to test and assess RF interface functionality and performance at various stages of development (Fig. 28). The surrogate SUT should be capable of emulating a variety of relevant radar waveforms. Surrogate SUT functionality can progress from operation at L-band, where RF interface can be tested in Nyquist Zone 1, to S-band for operation in the second Nyquist zone, and then to S/X/Ku-band with an up-/down-converter to assess RF interface performance across frequency. Surrogate SUT hardware should be reconfigurable for Rx, Tx, or Tx/Rx loopback testing with some signal-processing FPGA to provide a low-level simulated environment that incudes time delay and path loss to assess functionality.

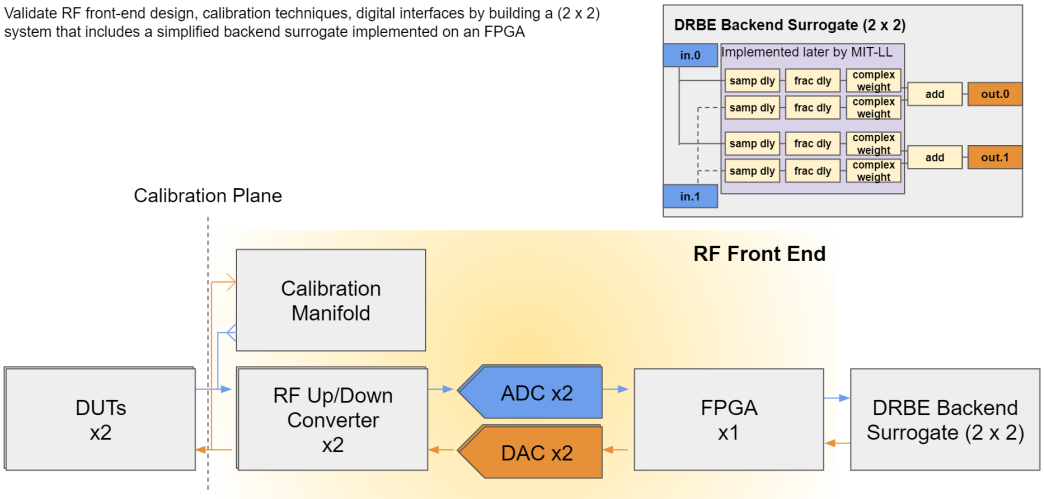


Fig. 28 Surrogate SUT RF interface test

12. Findings and Recommendations

The following six recommendations are proposed for consideration during the detailed design in Phase II of the program:

1. The RF interface should adopt a modular design approach to accommodate the wide range of SUTs envisioned, with primary focus on radar frequencies through Ku-band. Modular RF interface Options 1 and 2, shown in Figs. 5a and 5b, should be studied in the detailed design phase to understand the tradeoffs in performance and cost. If the non-wideband option is selected, the RF interface modules should be readily swappable among the RT-HPC ports to allow rapid reconfiguration to accommodate scenarios with different numbers of SUTs in each frequency band.

2. Proposed preliminary RF specifications:

   - Frequency coverage: 100 MHz to 18 GHz
   - IBW: 1 and 2 GHz should both be considered in the initial detailed design to accommodate different approaches for RT-HPC implementation.
   - Signal amplitude: Tx: –10 to +20 dBm from SUT; Rx: –90 to –40 dBm to SUT.
   - Latency: To be determined; maximum two-way latency (for minimum range) between SUT and RT-HPC is 800 ns. The RF interface hardware is not expected to contribute significantly to latency.

- Total no. of RF interfaces: approximately 20% of total DRBE ports with 2:1 ratio of Rx:Tx.

3. Selection of data converters should be coordinated with MIT-LL. The Xilinx RFSoC Gen 1 appears to be a good candidate and will be used for initial baseline design due to its capabilities, high level of integration, and maturity. Gen 3 Xilinx RFSoC should be evaluated to assess potential performance improvements over Gen 2.
4. Selection of the high-speed data converter clock source and distribution scheme should ensure fidelity and coherence across all RF interface channels. The data converter clock should be locked to DRBE system time reference.
5. BIST and end-to-end calibration should be included in the RF interface to assess the overall health of the system and ensure accuracy of the emulation.
6. Surrogate SUT radar hardware and environment processing development should be performed in parallel with the RF interface to enable testing and verification of RF interface functionality and performance.

13. Conclusions

This report summarizes some of the high-level requirements and specifications for the development of an RF interface for the DARPA DRBE program. It should serve as a guide for entering the detailed design phase and initial brass-board development to demonstrate interim capabilities toward meeting program goals. Additional refinements will be made as SUTs are identified and relevant specifications can be extracted to drive the RF interface design.

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List of Symbols, Abbreviations, and Acronyms

ADC	analog-to-digital converter
API	application programming interface
AWGN	additive white Gaussian noise
BAA	Broad Agency Announcement
BIST	built-in-self-test
BW	bandwidth
COTS	commercial off-the-shelf
DAC	digital-to-analog converter
DARPA	Defense Advanced Research Projects Agency
dBc	decibels relative to carrier
DC	direct current
DF	direction finding
DR	dynamic range
DRBE	Digital RF Battlespace Emulator
DRFM	digital RF memory
EA	electronic attack
EW	electronic warfare
FPGA	Field Programmable Gate Array
Gsps	giga-samples per second
HPA	high-power amplifier
IBW	instantaneous bandwidth
IF	intermediate frequency
IMD	intermodulation distortion
I/Q	in-phase/quadrature-phase
IEEE	Institute of Electrical and Electronics Engineers

ITU	International Telecommunications Union
LNA	low-noise amplifier
MIT-LL	Massachusetts Institute of Technology–Lincoln Laboratory
PA	power amplifier
PLL	phased lock loop
PRN	pseudo random noise
RF	radio frequency
RFSoC	RF system on chip
RMS	root mean square
RT-HPC	real-time high performance computer
Rx	receive
SAW	surface acoustic wave
SDR	software-defined radio
SFDR	spurious free dynamic range
SNR	signal-to-noise ratio
SQNR	signal-to-quantization-noise ratio
SUT	system under test
TWTA	travelling wave tube amplifier
Tx	transmit
USB	Universal Serial Bus

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